ZnO Nanowire Transistors

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Received: October 16, 2004; In Final Form: November 19, 2004

ZnO nanowire field-effect transistors (FETs) were fabricated and studied in vacuum and a variety of ambient gases from 5 to 300 K. In air, these *n*-type nanowire transistors have among the highest mobilities yet reported for ZnO FETs ($\mu_e = 13 \pm 5$ cm^2 V^{-1} s^{-1}), with carrier concentrations averaging $5.2 \pm 2.5 \times 10^{17}$ cm^{-3} and on−off current ratios ranging from 10^5 to 10^7. Four probe measurements show that the resistivity of the Ti/Au−ZnO contacts is 0.002−0.02 Ω·cm. The performance characteristics of the nanowire transistors are intimately tied to the presence and nature of adsorbed surface species. In addition, we describe a dynamic gate effect that seems to involve mobile surface charges and causes hysteresis in the transconductance, among other effects.

Introduction

ZnO is a wide band gap (~3.36 eV at 298 K) semiconductor with the wurtzite crystal structure. Over the past few years, a variety of gas-phase[1] and solution-phase[2,3] approaches have been devised to synthesize ZnO nanowires, tetrapods, combs, ribbons, and rings.[4−6] These ZnO nanomaterials have attracted considerable interest as room-temperature ultraviolet (UV) lasing cavities,[7] UV/visible photodetectors,[8,9] and active components in solar cells [10] and gas sensors.[11] However, the ability to reproducibly form high-quality ohmic contacts to ZnO remains a significant impediment to both the assessment of its intrinsic electronic properties (carrier type, mobility, and concentration) and its integration into complex nanoscale devices, such as light emitting diodes (LEDs) and electrically driven nanowire lasers. ZnO is intrinsically an *n*-type semiconductor, owing primarily to the presence of oxygen vacancies and/or zinc interstitials. There have been numerous reports of the synthesis of ZnO thin film transistors prepared by various types of sputtering. These transistors typically have field-effect mobilities ranging from 0.03 to 3 cm^2 V^{-1} s^{-1},[12−16] which is smaller than the Hall effect mobilities (100−205 cm^2 V^{-1} s^{-1})[17−19] reported for single crystals grown via vapor-phase transport or molecular beam epitaxy. There have been relatively few attempts to study the transport properties of single-crystals of ZnO as active FET channels. Arnold et al. reported the fabrication of FETs based on ZnO nanoribbons.[20] Also, Ng et al. fabricated ZnO nanowire transistors in a vertical geometry and found a mobility of ~0.5 cm^2 V^{-1} s^{-1}.[21] The transport properties of nanowire FETs made from other semiconducting nanowire materials have been previously studied. Recent reports have shown that the mobilities of p-Si[22] and n-GaN[23] nanowire FETs (560 cm^2 V^{-1} s^{-1} and 150−650 cm^2 V^{-1} s^{-1}, respectively) are comparable to or better than those of the highest quality thin-film devices.

Early studies of ZnO nanowire/ribbon device focused on their use as UV photodetectors.[8] These samples used Au contacts and were characterized by large contact resistances as a consequence of the Au−ZnO Schottky barrier (barrier height ~0.7 eV).[24] UV excitation of the nanowires increased their carrier concentration via direct electron−hole pair creation and the photodesorption of electron-trapping species from the nanowire surface.[25−27] Both processes allow higher currents to pass through the metal-semiconductor junction by tunneling and thermionic mechanisms.[28] This work suggests a pronounced effect of the nanowire surface on the conductivity and transistor properties.

Herein we report on the reproducible performance of single ZnO nanowire FETs in a standard global back-gate geometry. Using data from 20 different devices, we show that our average gas-phase ZnO nanowire transistors have among the highest reported mobility (μ) values reported for ZnO devices, $\mu = 13 \pm 5$ cm^2 V^{-1} s^{-1}, and have relatively low carrier concentrations of $5.2 \pm 2.5 \times 10^{17}$ cm^{-3} and on−off current ratios ranging from 10^5 to 10^7. Four probe measurements indicate our contact resistances to range from 2.1×10^{-3} to 1.6×10^{-2} Ω·cm^2. Additionally, we have observed a significant hysteresis and time-dependent shielding of the gate field.

Experimental Section

ZnO nanowires were synthesized using a carbothermal reduction process at 900 °C with a gold thin film as the catalyst.[7] TEM studies show that the wires are single crystals with the wurtzite structure and have diameters ranging from 50 to 200 nm and lengths up to 10 μm. The as-made wires have well-faceted hexagonal cross-sections with {100} faces and grow along the [001] direction. They also lack an amorphous outer coating that might complicate the formation of ohmic metal-semiconductor contacts. They were dispersed in VLSI grade 2-propanol and transferred onto degeneratively doped Si(100) wafers coated with 600 nm of thermal oxide, ($\rho = 0.008 - 0.02$ Ω·cm, Sb dopant, Silicon Quest International), which had prefabricated Cr/Au probe pads patterned by optical lithography.

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Electron-beam lithography was used to define contacts between the nanowires and the existing probe pads. Ti/Au (200 nm/50 nm) contacts were deposited via electron beam evaporation. Immediately preceding metal deposition, the samples were cleaned in a 50 W O_2 plasma for 60 s to obtain ohmic devices. Shorter plasma times were found to produce devices with much larger contact resistances and/or nonlinear $I-V$ behavior. After liftoff, the samples were annealed at 200−400 °C in O_2 to further lower the contact resistance.

Transistor measurements were performed using a home-built probe station equipped with a HP 4156B semiconductor parameter analyzer. Current values were obtained using two different integration times: 2 s per point for currents less than 10^{-10} Å and 0.1 s per point for currents greater than 10^{-10} Å. All current−voltage traces were taken from negative to positive V_{sd} or V_G. The samples were also wire-bonded onto a 16-pin die and measured in a Janis ST-500 cryostat equipped with a Keithley 236 source-measure unit, a Keithley 230 voltage source and a gas manifold for environmental control. The cryostat base pressure was 1×10^{-5} Torr. UV excitation was provided by a HeCd laser operating at 325 nm.

Results and Discussion

Figure 1a is a scanning electron microscope (SEM) image of a typical ZnO nanowire FET. A current−voltage plot of the same device (Figure 1b) shows the pronounced gate effect indicative of an *n*-type semiconductor with a moderate carrier concentration. In general, the I_{sd} vs V_{sd} curves are linear out to 2 V, suggesting that the wire-electrode contact is ohmic. The current saturation in positive bias does not reverse when switching the source and drain electrodes, or sweeping V_{sd} from positive to negative and is typical behavior for n-doped FET devices.[28] To determine the efficiency of the gating behavior, transconductance measurements (I_{sd} vs V_G) were obtained at a variety of V_{sd} values (Figure 1c). The threshold voltage for current onset (V_{th}) is −12.5 V for this device and varied from −4.5 to −28 V across the twenty samples. At more negative gate voltages there is no measurable current through the wire. Note that the V_{th} is averaged for all V_{sd} values. At larger V_G values the current linearly increases with respect to gate voltage. The on−off current ratio (I_{ON}/I_{OFF}) of $>10^5$ is deduced by plotting the current on a logarithmic plot (Inset in Figure 1c).

From the transconductance plots, the mobility of our nanowire devices can be estimated using

$$\frac{dI_{sd}}{dV_G} = \frac{\mu C}{L^2} \tag{1}$$

where μ is the carrier mobility, C is the capacitance, and L is the length of the active nanowire channel. The capacitance is given by

$$C = \frac{2\pi\epsilon_0\epsilon_{SiO_2}L}{\ln\left(\frac{4h}{d}\right)} \tag{2}$$

where ϵ_{SiO_2} is the dielectric constant of the gate SiO_2, h is its thickness, and d is the wire diameter. The carrier concentration (n_e) is likewise calculated from

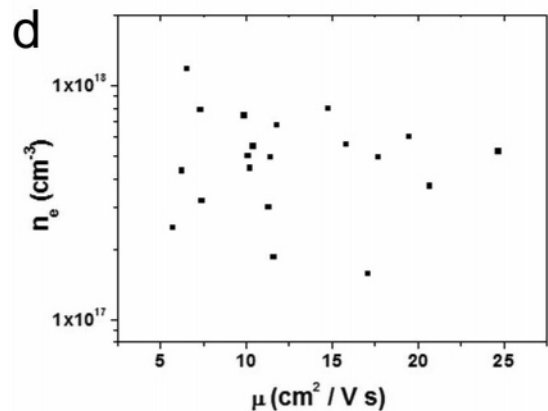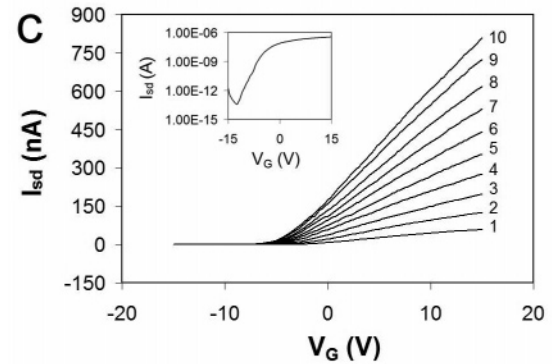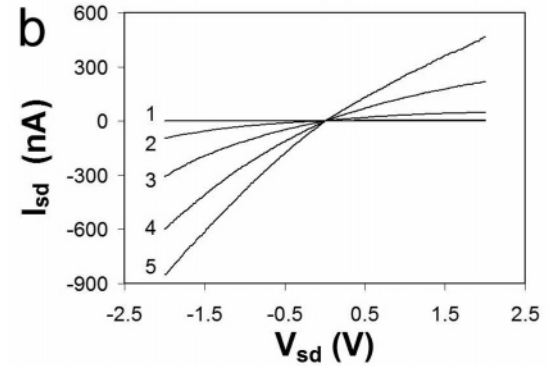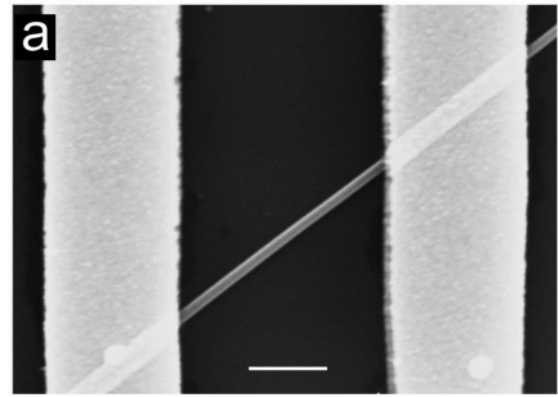$$n_e = \frac{V_{th}C}{q\pi\left(\frac{d}{2}\right)^2 L} \tag{3}$$

Figure 1. (a) SEM micrograph of a 101 nm diameter ZnO nanowire device (scale bar = 1 μm). (b) Current (I_{sd}) vs voltage (V_{sd}) curves recorded at different gate voltages for the device shown in (a). Curves 1−5 correspond to gate voltages of −10, −5, 0, +5, and +10 V, respectively. (c) Current (I_{sd}) vs gate voltage (V_G) of the same device measured at bias voltages from 0.1 to 1.0 V. Curves 1−10 correspond to bias voltages of 0.1, 0.2, 0.3, 0.4, 0.5, 0.6, 0.7, 0.8, 0.9, and 1.0 V, respectively. The inset plots the current (I_{sd}) vs gate voltage (V_G) measured at a bias voltage of $0.5V_{sd}$ on a logarithmic scale. (d) Carrier concentration (n_e) vs mobility (μ) for all transistor devices fabricated.
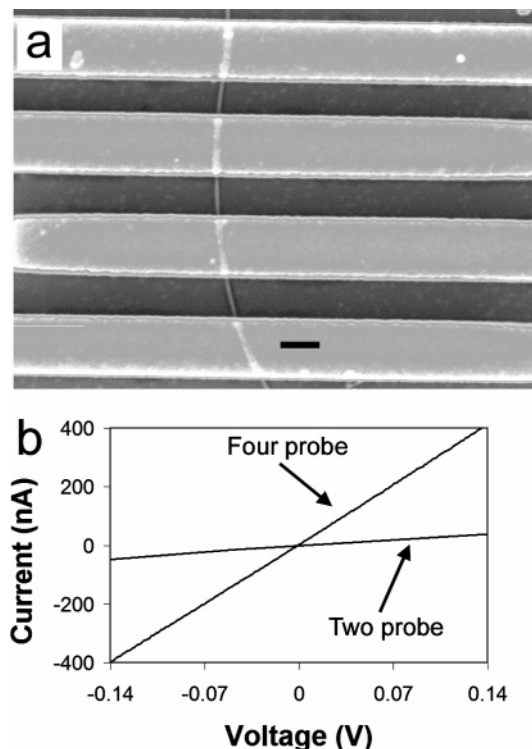
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Figure 2. SEM micrograph of a four-probe device with a diameter of 178 nm (scale bar = 1 μm). (b) $I-V$ curves measured in a two-probe and four-probe configurations.

The FET shown in Figure 1 has a mobility of 17.1 cm^2 V^{-1} s^{-1} and a carrier concentration of 1.1×10^{17} cm^{-3}. Figure 1d is a plot of the n_e vs μ for all 20 devices. The average mobility and carrier concentration are 13 ± 5 cm^2 V^{-1} s^{-1} and $5.2 \pm 2.5 \times 10^{17}$ cm^{-3}. The I_{ON}/I_{OFF} ranged from 10^5 to 10^7 for these nanowire FETs.

We have also fabricated FETs in a four-probe configuration (Figure 2a shows an SEM image) to determine the resistance of the Ti/Au contacts (R_C). The contact resistance is determined by comparing resistance values for the two-probe (R_{2P}) and four-probe (R_{4P}) geometries according to

$$2R_C + R_{4P} = R_{2P} \qquad (4)$$

Figure 2b compares the two-probe (middle electrodes) and four-probe $I-V$ plots for a single device. By multiplying R_C by the nanowire surface area in the contact region, assuming a cylindrical wire, we find a contact resistivity of 2.1×10^{-3} to 1.6×10^{-2} $\Omega \cdot$cm^2. These values are similar to those reported for Ti/Au contacts in thin films.[29] In general, the contact resistance is 2–10 times the resistance of the nanowire. Lower contact resistances for ZnO thin films have been reported in the literature using more complex multilayer metal contact schemes.[30,31]

The dependence of nanowire FET performance on temperature was studied for a smaller number of samples. Figure 3a is a sequence of $I-V$ traces taken from 25 to 300 K. We find that the wire conductivity decreases upon cooling, due to a lower carrier concentration and an increase in contact resistance. The device in Figure 3a becomes nonohmic near 150 K, as fewer carriers have enough thermal energy to overcome the interface barrier height. The inset in Figure 3 better illustrates this nonohmicity by plotting I_{sd} vs V_{sd} at 4.5 K. The estimated μ and n_e at each temperature is plotted in Figures 3b,c, respectively. The carrier concentration decreases upon cooling, as is expected for semiconductor materials. Also, the electron mobil-
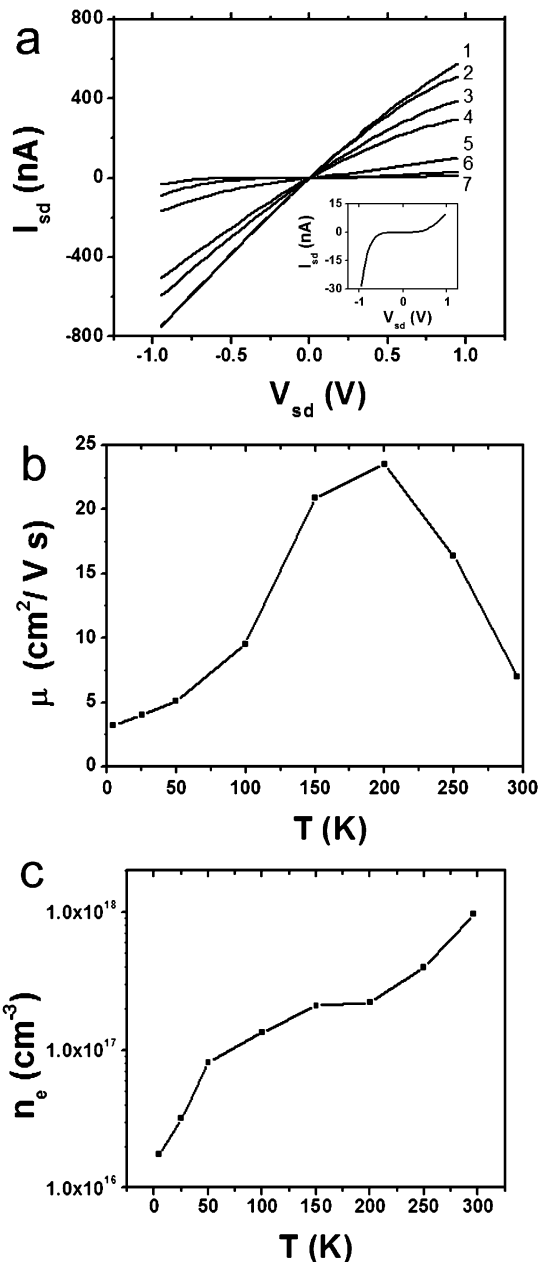

Figure 3. (a) Temperature-dependent I_{sd} vs V_{sd} data for a 116 nm device. Curves 1–7 correspond to measurements obtained at 296, 250, 200, 150, 100, 50, and 25 K, respectively ($V_G = 0$ V). The inset plots the I_{sd} vs V_{sd} measurement obtained at 4.5 K. Temperature-dependent mobility (b) and carrier concentration (c) obtained for this device. Lines are drawn in (b) and (c) to guide the eye.

ity of this device increases upon reducing the temperature until it reaches a maximum at 150 K. This increase upon cooling is expected in semiconductors due to a lower electron–phonon scattering rate, caused by freezing out of phonons, and a lower electron–electron scattering caused by a decrease in the carrier concentration.[32] Additionally, the semiconductor mobility is expected to decrease, approaching 0 K, as carrier scattering due to the presence of ionized impurities predominates. Yet, the measured values of n_e and μ are dependent not only on the fundamental semiconductor mobility but also the device geometry and the contact resistance, therefore making deductions about the relative concentrations of electronic scattering due to phonons and ionized impurities difficult.

During our experiments, we noticed that the change in I_{sd} induced by the gate potential eventually dissipated after
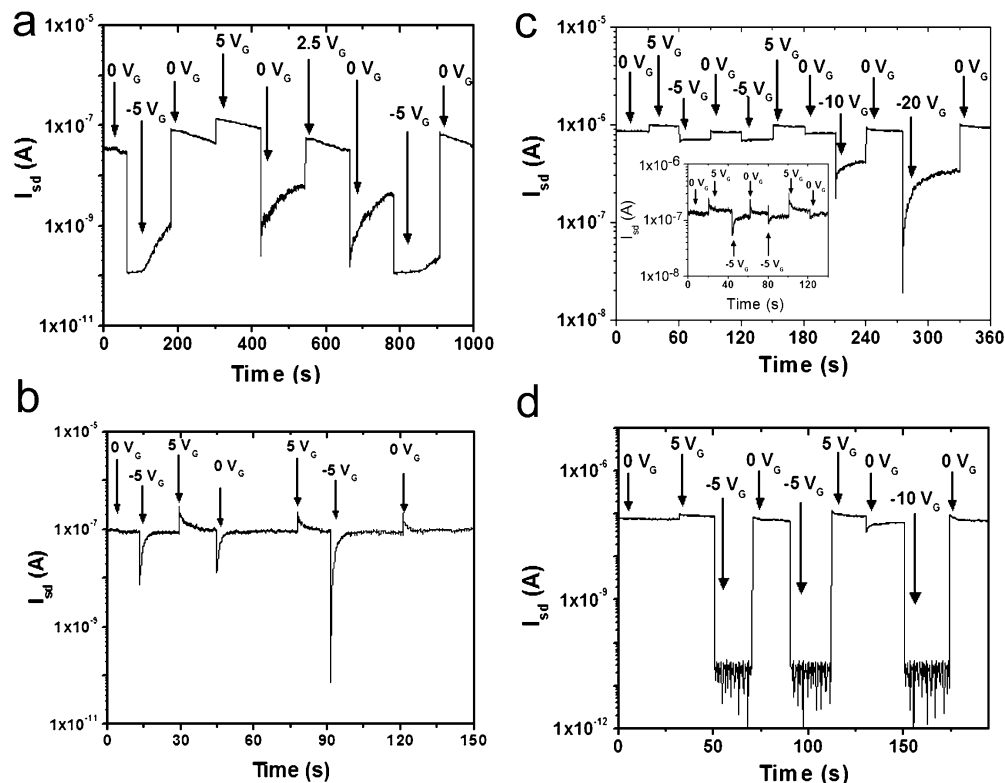
Figure 4. (a) I_{sd} vs time ($0.4V_{sd}$) at different gate voltages. The assigned gate voltage is switched on at each data spike and held until the next ascribed gate voltage. (b) I_{sd} vs time ($1.0V_{sd}$) for the nanowire FET with the quickest rate of current dissipation. (c) I_{sd} vs time ($1.0V_{sd}$) for the device shown in (b) measured at 1×10^{-5} Torr. The inset plots the I_{sd} vs time for the same nanowire immediately after reexposing the sample to air at atmospheric pressure. (d) I_{sd} vs time ($1.0V_{sd}$) for the device shown in (b) obtained 30 min after cleaning the nanowire surface for 5 min with a HeCd laser in dry flowing O_2.

prolonged gating. This effect is best illustrated by monitoring the current as a function of time by varying V_G under a constant V_{sd}, such as the time traces shown in Figure 4a. As the gate voltage is altered, a coinciding spike in the current results but decays quasi-exponentially. This gate screening not only causes the I_{sd} to decay to the 0 V_G level, but also spikes in the opposite direction to the gate voltage immediately preceding it. Specifically, if the preceding gate voltage was lower (higher), then the current will spike in the positive (negative) direction upon switching the gate voltage. Furthermore, the current reading immediately after the switch significantly depends on the preceding gate voltage value (Figure 4a,b). This rate of current decay in this FET is typical for most devices fabricated. There is no apparent correlation between the rate of current decay and any physical property of the nanowire (i.e., diameter, length, etc.) or electrode placement. A time trace of the FET with the quickest rate of current decay is shown in Figure 4b. This extremely rapid decay is well-suited for the qualitative comparison to be discussed below.

To determine the role that adsorbed species on or near the surface of the ZnO nanowires on the time-dependent behavior of the gate voltage, the devices were measured after being held in a vacuum ($\sim 1 \times 10^{-5}$ Torr) for 1 h. The conductance increased by a factor of 2−5 for all devices measured, which is indicative of the desorption of electron-trapping surface species. In a vacuum, the devices exhibited a much weaker and slower dynamic gating effect (Figure 4c). Backfilling the chamber with laboratory air resulted in a reversion to the original behavior (inset). This suggests that the presence of adsorbed surface species plays a strong role in the hysteresis and time-dependent gate dissipation of the data.

Thermal desorption[33] and UV photodesorption[25,26] in a vacuum are two methods that have been previously reported to

clean ZnO surfaces. The influence of both of these cleaning techniques on the transistor properties for three ZnO FET devices has been studied. In these experiments, the FETs were held under a vacuum for 1 h before the devices were irradiated with UV light for a period of 5 min. IV and transconductance measurements were obtained under vacuum five minutes after the irradiation treatment was complete. UV irradiation of the nanowire FETs using a 254 nm handheld UV source resulted in a decrease in the average mobility of these devices from 12 ± 4 cm^2 V^{-1} s^{-1} (value in air) to 5 ± 4 cm^2 V^{-1} s^{-1}, an increase in the average carrier concentration from $3.7 \pm 1.8 \times 10^{17}$ cm^{-3} to $2.4 \pm 1.5 \times 10^{18}$ cm^{-3}, and a decrease in the average resistivity from 8.4 ± 6.4 Ω·cm to 0.36 ± 0.26 Ω·cm from the values originally derived from measurements in air. Consequently, the measured resistivity of the wire decreases as surface conduction is enhanced, and the device mobility decreases due to increased carrier−carrier scattering. UV irradiation using a higher power continuous wave HeCd laser resulted in a further decrease in resistivity to 0.037−0.20 Ω·cm. No gating behavior was observed, as is expected with a further increase in carrier concentration in conjunction with a greater removal of surface species. An alternative method of cleaning ZnO surfaces is to anneal the devices in a vacuum under 150 °C. This heating treatment has been previously shown to remove H_2O, CO, and CO_2 species from ZnO thin films.[33] The same three devices were annealed at 150 °C under vacuum for 2 h. Subsequent $I−V$ and transconductance measurements were obtained after cooling to room temperature. After treatment, the nanowire FETs showed mobilities of 3−26 cm^2 V^{-1} s^{-1}, a carrier concentration of $1.8−8.7 \times 10^{18}$ cm^{-3}, and a resistivity of 0.19 ± 0.06 Ω·cm. This treatment does not produce a statistically significant difference in the mobility as compared to the values measured in air. However, there was a lower room-

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TABLE 1: Mobility, Carrier Concentration, and Resistivity of a 116 nm Diameter Nanowire FET Measured in an Environmental Cell Filled with a Variety of Atmospheres[a]

	μ [cm^2/(V s)]	n_e (cm^{-3})	ρ (Ω cm)
air	10.1	5.3×10^{17}	4.37
dry O$_2$	18.2	1.74×10^{17}	1.88
dry N$_2$	6.13	2.4×10^{18}	0.422
vacuum	6.99	9.6×10^{17}	0.93

[a] These values were obtained from measurements taken 15 min after the surface of the nanowire was cleaned with 5 min of UV irradiation from a He:Cd laser. The cell was continually flushed with the above atmospheres during all measurements.

temperature resistivity and a higher room-temperature carrier concentration after treatment, similar to what was observed with phototreatment. For these particular devices, UV laser photodesorption is the most efficient process for removing electron-withdrawing and other various surface species from the ZnO nanowires.

To further probe the influence of surface species (i.e., water, oxygen, etc.) on the transport properties and dynamic gate effect of the devices, measurements were taken in dry N$_2$, dry O$_2$, and vacuum. Before measurement, the nanowires were exposed to the desired ambient for at least 2 h and then cleaned by UV photodesorption for 5 min. The I_{sd} vs V_{sd} data were collected 15 min after irradiation. Table 1 gives the estimated n_e, μ, and ρ measured in air, dry O$_2$, and dry N$_2$, and under vacuum for the same wire measured in Figure 4b. Under vacuum and N$_2$ (post UV illumination), the n_e increased by a factor of 2–4. This rise in n_e is most likely caused by the thinning of the depletion layer in the less oxidized outer surface after UV illumination. Furthermore, the mobility decreases by 30% to 40%. This is likely due to an increase of electron–electron scattering in the surface and near surface (nonflat band region) of the nanowires as well as an increase in shielding of the gate voltage from the inner nanowire by the metallic outer surface. Naturally, the trend reverses when an electronegative species is bound to the surface of the nanowire, as is observed when the nanowire is measured under an O$_2$ ambient. In this case, the n_e shows a decrease by about a factor of 3, and the mobility almost doubles. Yet, the higher resistivity of the nanowire in air, rather than in O$_2$, suggests that another oxidative species might be present bound to or near the surface of the nanowire (e.g., water) and plays a significant role in determining the overall properties. Finally, there is a marked decrease in the rate of gate voltage dissipation when the nanowires are maintained in a dry O$_2$ environment. Figure 4d is the time trace of the device plotted in Figure 4b in dry O$_2$. These data suggest the gate voltage dissipation is not due to the influence of O$_2$ absorbed on the surface. Overall, this illustrates the dependence of the measured transistor properties of these nanowire FETs on the presence of adsorbed surface species.

The dependence of the atmosphere on the rate of the gate voltage dissipation suggests that this effect is a real phenomenon in our nanowires, and not a measurement error due to capacitive coupling leakage between the gate electrode and the source/drain electrodes. Additionally, the I_{sd} remains constant at the noise level when the gate voltage is switched without the presence of a nanowire between the two electrodes. This phenomenon has been previously reported for SnO$_2$ nanoribbon devices and was suggested to occur due to the presence of charged species at or near the surface of the nanowire.[34] Furthermore, the influence of charged or neutral adsorbed molecules and has been previously observed to play a dramatic role on the transport properties of Ge nanowires,[35] Si nano-

wires,[22,36,37] carbon nanotubes[38,39] and metal oxides.[40–43] Hysteresis behavior is commonly seen in carbon nanotube FETs and has been attributed to the capacitive charging of water species that are weakly adsorbed to the nanotube and to silanol groups on the SiO$_2$ dielectric that are near the surface of the nanotube. In our ZnO nanowire FETs, the observed reduction of the hysteresis and time-dependent shielding behavior in a dry O$_2$ environment suggests a similar effect is occurring in our system. Nevertheless, a thorough systematic investigation is required to pinpoint the exact physical and chemical explanations for these phenomena.

Conclusions

Twenty ZnO nanowire FET devices have been fabricated, and their transport properties have been characterized. The role of bound surface species has been found to play an important role on the transport properties of the devices, specifically on stabilizing or destabilizing the surface and ultimately the ability to dissipate charge across the nanowire. It is interesting to note that the nanowires that were studied here have diameters in the range 80–200 nm, which is much larger than the estimated Debye length in ZnO of 20–50 nm.[44] Yet there remains a significant overall influence of the surface chemistry on the transport properties of these devices. The physical nature of the gate voltage shielding, the chemical identity of the surface species that lead to this dissipation, and the effect of a passivating dielectric layer are all questions that necessitate further study.

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