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Si Nanowire Bridges in Microtrenches: Integration of Growth into Device Fabrication**

By *Rongrui He*, *Di Gao*, *Rong Fan*, *Allon I. Hochbaum*, *Carlo Carraro*, *Roya Maboudian*, and *Peidong Yang**

Silicon nanowires are attractive building blocks for nanoscale electronic systems due to their compatibility with existing semiconductor technology. Studies have focused on their synthesis,[1–5] with considerable advances made in the control of structures,[6] electrical,[7,8] and thermal[9] properties. For practical applications, different strategies have been explored to fabricate nanowire-based devices. The pick-and-place approach[7,8,9] has succeeded in making individual devices such

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[**] This work was supported by the National Science Foundation (NIRT grant # DMI-0304209). P. Y. is an Alfred P. Sloan Research Fellow. Work at the Lawrence Berkeley National Laboratory was supported by the Office of Science, Basic Energy Sciences, Division of Materials Science of the U. S. Department of Energy. We thank the National Center for Electron Microscopy for the use of their facilities.

 © 2005 WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim DOI: 10.1002/adma.200401959

as field-effect transistors (FETs), isolated thermal bridges, and chemical sensors, but it is time-consuming and unsuitable for large-scale manufacturing. The Langmuir–Blodgett technique has been utilized as a powerful and low-cost approach to align nanowires[10] and make large-scale arrays of devices,[11] showing a significant advance towards nanowire-based integrated circuits. However, in some circumstances, instead of following the "bottom–up synthesis first, assembly and top–down fabrication next" approach, it is desirable to grow nanowires precisely and rationally in predetermined device architectures.[12] Direct integration of growth into fabrication will markedly simplify procedures and avoid deterioration of nanowires in some micro-/nanofabrication processes. In the study reported here, Si nanowires have been grown laterally in microtrenches that were prefabricated on silicon-on-insulator (SOI) wafers, demonstrating that nanowire growth and device fabrication can be achieved simultaneously. Lateral bridging growth was first demonstrated for GaAs nanowires[13] and recently for Si nanowires.[14] However, well-controlled growth and device operation were not achieved. In this paper, we demonstrate excellent epitaxial growth of bridging Si nanowires and effective control of diameters, lengths, and densities. Electrical measurements show that the nanowires in trenches could serve as versatile active components in circuits.

The idea of nanowire-in-trench structures is based on epitaxial growth of Si nanowires. Si nanowires grow preferentially along <111> directions.[3,6,15] If the vertical {111} planes contained in a Si(110) wafer are exposed by vertical etching, Si nanowires can be grown laterally, bridging the two face-to-face {111} surfaces, as illustrated in Figure 1A. In the detailed procedure, we started with a heavily doped Si(110) SOI wafer. Trenches were microfabricated photolithographically by proper alignment of the substrate and the pattern, so that the {111} planes were exposed. Figure 1B shows a scanning electron microscopy (SEM) image of a group of parallel trenches obtained. After making trenches, Au clusters were dispersed on the substrate as catalysts for vapor–liquid–solid (VLS)[3] growth of nanowires carried out in a subsequent chemical vapor deposition (CVD) process using $SiCl_4$ as the precursor. It is expected that when a growing nanowire impinges on the opposite sidewall, an electrical or thermal connection will be automatically made, with the bridging Si nanowire being the active unit, the Si pads confining the trench as the electrodes, and the SiO_2 layer underneath acting as the insulator/dielectric barrier. Figure 1C shows the SEM image of such a structure. Two nanowires, each with a diameter of ~80 nm, have bridged the 2 μm wide $(1\bar{1}\bar{1})$ trench, and one nanowire has bridged the $(1\bar{1}1)$ trench. The excellent epitaxy and interface cleanliness shown here are the two advantages of the CVD process based on $SiCl_4$ precursor and Au clusters. These are crucial for obtaining devices with high quality.

These two features can be examined in more detail in Figure 2. Epitaxial growth, as the foundation of this work, is discussed first. For the samples shown in Figure 2, the SiO_2 mask used in photolithography to form the trenches was removed before growth to allow the nanowires to grow on the top exposed Si(110) surfaces. As shown in Figure 2A, besides perpendicular growth of nanowires on the {111} vertical surfaces as expected, well-aligned nanowires also grew along the $[11\bar{1}]$ and [111] directions on the (110) top surface. Similar results were obtained in the epitaxial growth of GaAs nanowires.[16] Moreover, surface roughness had little influence on epitaxy. In the magnified image of the vertical {111} surface (Fig. 2C), scalloping of the surface, which was caused by the deep reactive-ion etching[17] (DRIE) cycles during microfabrication of the trenches, is noticeable. Nonetheless, nanowires persisted in growing along the <111> directions without much influence from the local variation of surface orientation. One can conclude that the epitaxially grown Si nanowires are always aligned with the crystallographic <111> directions, with the

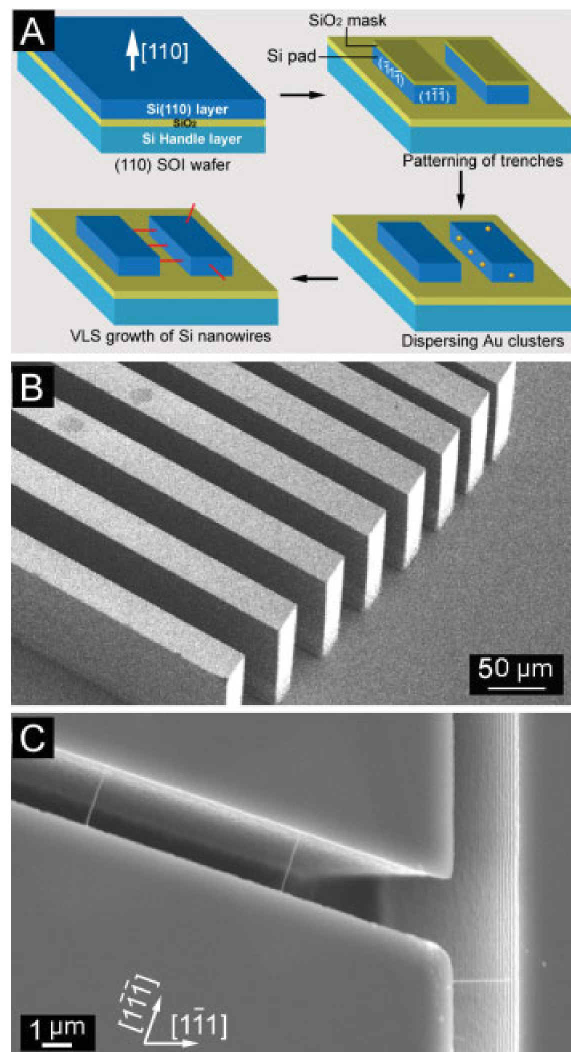

Figure 1. Overall process for growth of Si nanowire bridges in microfabricated trenches. A) Schematic illustration of the fabrication of the Si nanowire bridge between two vertical Si{111} surfaces on (110)-oriented SOI wafers. B) SEM image of a group of parallel trenches formed on an SOI wafer. C) SEM image of nanowire bridges grown in the microtrenches.

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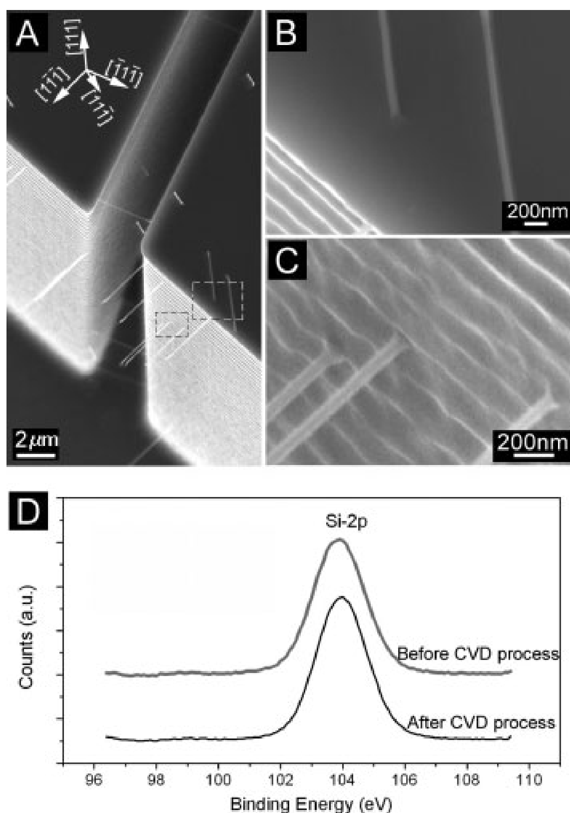

Figure 2. Epitaxial alignment and interface cleanliness for Si nanowire growth in microtrenches. A) <111> crystallographic alignment is exhibited on both Si{111} and {110} surfaces. Crystallographic geometry is illustrated by the projection of four <111> vectors. Further magnified images for the areas demarcated by the rectangular frames are shown in (B) and (C). D) X-ray photoelectron spectra of Si 2p regions taken from the insulating SiO_2 surface before and after the 30 min CVD process.

local orientation of the substrate only affecting which specific <111> direction the nanowires prefer (e.g., nanowires prefer the perpendicular [111] direction for a relatively smooth (111) surface). This alignment is believed to be driven by the energetically favorable <111> growth and facilitated by crystallization at the liquid–solid interface in the VLS process. Here, we stress the uniqueness of our $SiCl_4$-based CVD synthesis, because no epitaxial alignment as significant as that shown here has been observed in other synthesis methods, such as pulsed laser deposition, thermal evaporation of SiO_2, and SiH_4 CVD.[1,2] This robust tendency for Si nanowires to align along the <111> directions simplifies device fabrication processes, e.g., by reducing such requirements as alignment for etching (to find <111> directions precisely) and polishing of surfaces.

Thin-film deposition is a process that might occur simultaneously with VLS growth of nanowires in CVD. To prevent potential current leakage through an unintentionally deposited Si film, this film deposition must be minimized, especially on the insulating SiO_2 surfaces. The growth conditions chosen in the present work ensure that the deposition rate of thin films is negligible during VLS growth. For example, there was no observable deposition besides nanowire deposition on the Si(110) surface (Fig. 2B), or on the Si$(1\bar{1}\bar{1})$ surface (Fig. 2C). More quantitative results were obtained by X-ray photoelectron spectroscopy (XPS), a surface-sensitive characterization technique. As shown in Figure 2D, there are no differences between the two Si 2p spectra taken from SiO_2 surface before and after the thirty-minute CVD process. Only the chemically shifted Si 2p peaks characteristic of SiO_2 are observed at 103.8 eV, while the Si 2p peaks of elemental Si at 99.8 eV are absent (the standard Si 2p peak is 103.3 eV for SiO_2, and 99.3 eV for Si[18]). The large difference in deposition rates between the thin films and nanowires is attributed to the catalytic action of liquid droplets in the VLS growth.[19] Furthermore, in $SiCl_4$ CVD, thin-film growth is further suppressed by the well-documented etching effect of Cl species generated at high temperatures.[20,21]

For device applications, it is important to ascertain the connections between the Si nanowires and the sidewalls. This issue was investigated in over-grown nanowires whose lengths exceeded the widths of the trenches. Figure 3 shows a sample in which nanowires with average lengths of 4 μm were grown in 2 μm wide trenches. Nanowires 1 and 2, located in different

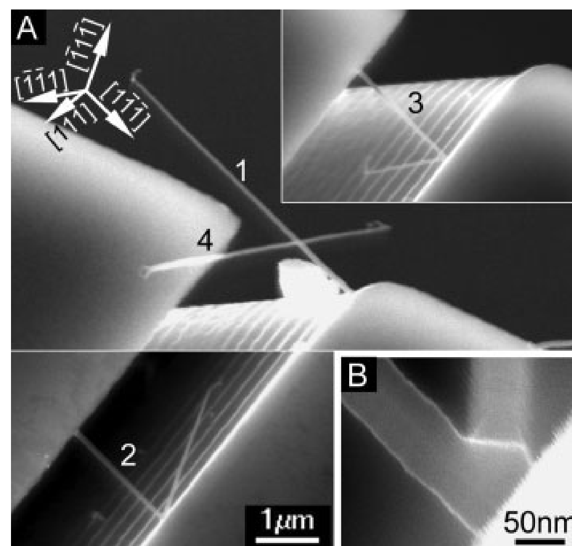

Figure 3. Connections between the Si nanowires and the trench sidewalls. A) Nanowire 1 (which grew straightly along the $[\bar{1}11]$ direction) and Nanowires 2 and 3 (which grew along $[1\bar{1}\bar{1}]$) developed backwards, growing along $[\bar{1}1\bar{1}]$ and $[\bar{1}\bar{1}1]$, respectively, after being blocked by the opposite walls. B) A magnified view of the wire–sidewall interface.

positions of a trench, and Nanowire 3, located in another trench, are arranged together for easy comparison (Fig. 3A). Nanowire 1 grew straight along the $[\bar{1}11]$ direction with no blockage, and is used as a reference for the other two. Nanowires 2 and 3, which grew along the $[1\bar{1}\bar{1}]$[22] direction, reached the opposite $(\bar{1}11)$ walls but continued to grow backward with the gold catalysts still on their tips. The backward growth directions were determined to still be <111> exclusively, by extensive measurements of the angles and compari-

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son with the nanowires grown on the (110) surface. There are three possible backward directions for a given nanowire. Specifically, they are, [111], $[\bar{1}1\bar{1}]$ (Nanowire 2), and $[\bar{1}\bar{1}1]$ (Nanowire 3) for a nanowire originally growing along the $[1\bar{1}\bar{1}]$ direction. This observation is consistent with the <111> alignment in epitaxy discussed above. The mechanism of backward growth directly indicates that nanowires should be self-welded with the opposite sidewalls and should form solid connections, as shown in Figure 3B. The mechanical rigidity was further confirmed in the nanowire deflection experiments carried out using atomic force microscopy, which will be reported elsewhere. The connections shown here are different from disk formation reported previously[14] possibly because of the different growth conditions used, such as the presence of precursor molecules and the temperature.

The rational fabrication of nanowire devices requires tight control of the diameters, lengths, and densities of the nanowires. Such control can be achieved in the Au-cluster-catalyzed growth. First, the lengths of the nanowires can be tailored to fit in trenches of varying widths by controlling the growth time. For instance, Figure 4A shows four bridging nanowires with similar diameters (~75 nm) that have lengths of 1.5, 2.5, 4, and 10 μm respectively. Second, the diameters of the nanowires can be defined by the sizes of the Au clusters.

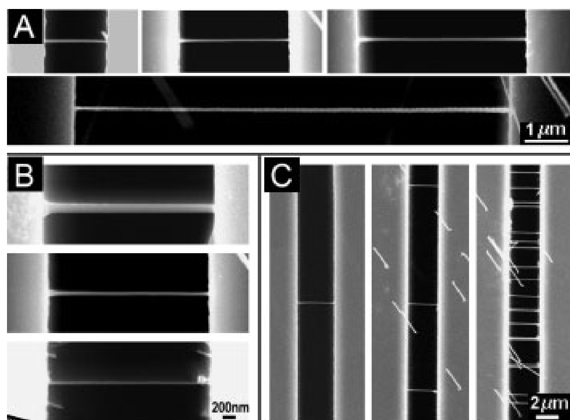

Figure 4. Control of length (A), diameter (B), and density (C) of bridging Si nanowires. A) The lengths of the four nanowires with similar diameters of ~75 nm are 1.5, 2.5, 4, and 10 μm, respectively. B) The diameters of the three nanowires are 140, 70, and 35 nm from top to bottom. C) The densities are 1 wire per 50 μm, 4 wires per 50 μm, and 40 wires per 50 μm from left to right.

As shown in Figure 4B, the diameters of nanowires grown from 100, 50, and 10 nm Au clusters are 140, 70, and 35 nm, respectively. Finally, the density of nanowires in the trenches can be controlled by the surface density of the Au clusters. In the example shown in Figure 4C, densities of 1 wire per 50 μm, 4 wires per 50 μm, and 40 wires per 50 μm were obtained by using a series of diluted Au colloids. It is worth pointing out that nanowire diameter cannot be controlled independently of nanowire density in thin-film-catalyzed nanowire growth, where a decrease in diameter is always accompanied by a decrease in density.[23] In contrast, in Au-cluster-catalyzed growth, diameters and densities can be controlled independently.

The capability to flow current through the bridging nanowires using the Si pads as electrodes provides the basis for the applications of nanowire-in-trench structures in nanoscale electronics. We demonstrated the electrical connectivity in a simple network consisting of five Si pads connected by bridging nanowires (Fig. 5A). Two tungsten probes were directly placed on top of the pads to perform electrical-transport measurements. The results are shown in Figure 5B. The current–

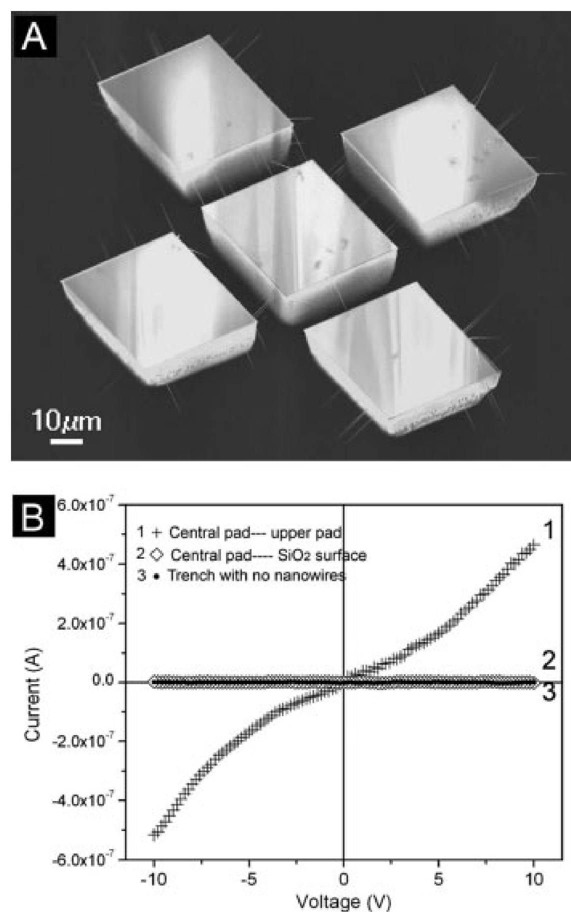

Figure 5. Electrical-transport measurements on nanowire-in-trench structures. A) SEM image of a network consisting of five Si pads connected by bridging Si nanowires. B) *I–V* curves measured using tungsten probes.

voltage (*I–V*) curve, curve 1, shows the measurement between the central pad and upper pad with several nanowires in between, indicating current flow through the nanowires. Curve 2 is the *I–V* curve measured between the central pad and SiO_2 layer underneath, and curve 3 is that measured on a trench with no bridging nanowires. No currents were measured in these cases, consistent with the XPS results, indicating that transport occurred exclusively through nanowire bridges. Furthermore, contact problems existing in the current "fabri-

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cating electrodes after growth" approach (e.g., the deterioration of the electrode–nanowire interface) are avoided here, since the electrodes and nanowires are integrated into one single crystalline piece in the bridge structures. More advanced functions can be realized by further modification of the prototype devices shown here.

In conclusion, we have demonstrated direct integration of nanowire growth into device fabrication by bridging Si nanowires in microfabricated trenches, which puts both growth and fabrication on a more rational and simple path towards nanowire-based integrated circuits. The framework of the devices can be pre-defined in top–down fabrication before growth, and structures of the core units, i.e., the nanowires, can be readily realized using the Au-cluster-catalyzed $SiCl_4$ CVD synthesis. These new control capabilities make the nanowire-in-trench strategy desirable for various applications, such as chemical sensors, FETs, and nanomechanical resonators.

Experimental

Fabrication of Trenches: (110) SOI wafers used in the study consisted of a 20–80 μm thick Si(110) layer, a 0.5–2 μm thick thermally grown SiO_2 layer, and a ~400 μm thick Si(100) handle layer. A thermal SiO_2 film 0.5–1 μm in thickness was first grown on a Si(110) surface in H_2O vapor at 1050 °C. Patterns designed for trenches were made on spin-coated photoresist by photolithography and then transferred onto the SiO_2 layer by plasma etching. Using the patterned SiO_2 film as mask, the DRIE process was carried out to etch the Si(110) layer, so as to expose vertical {111} planes in an inductively coupled plasma etcher (Surface Technology Systems). Trenches formed after etching reached the insulating SiO_2 layer of the SOI wafer.

Growth of Si Nanowires: In some cases, the SiO_2 mask was etched in 10 % HF before growth for studying the epitaxy or for better imaging, while in other cases, it was etched after growth to remove the nanowires on the top surfaces. For dispersion of Au clusters, a drop of 0.1 wt.-% poly-L-lysine (Ted Pella, Inc.) was first deposited on the surface of the substrate, followed by rinsing with de-ionized (DI) water and drying in N_2. Then a drop of Au colloids (Ted Pella, Inc.) was dispersed on the substrate, which was also followed by rinsing with DI water and drying in N_2. The synthesis was carried in a horizontal hot-wall furnace at 800–850 °C. $SiCl_4$ was used as precursor and 10 % H_2 in Ar was used as both the carrier and diluted gas.

Characterization: All the images were taken by a JEOL-6400 field-emission scanning electron microscope. X-ray photoelectron spectra were obtained in an ultrahigh vacuum chamber equipped with an Omicron EA125 electron energy analyzer and an Omicron DAR400 X-ray source. Binding-energy values were corrected using the C 1s peak as reference.

Received: December 1, 2004
Final version: March 15, 2005
Published online: April 20, 2005

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