Giant piezoresistance effect in silicon nanowires

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The piezoresistance effect of silicon[1] has been widely used in mechanical sensors[2–4], and is now being actively explored in order to improve the performance of silicon transistors[5,6]. In fact, strain engineering is now considered to be one of the most promising strategies for developing high-performance sub-10-nm silicon devices[7]. Interesting electromechanical properties have been observed in carbon nanotubes[8,9]. In this paper we report that Si nanowires possess an unusually large piezoresistance effect compared with bulk. For example, the longitudinal piezoresistance coefficient along the ⟨111⟩ direction increases with decreasing diameter for p-type Si nanowires, reaching as high as $-3{,}550 \times 10^{-11}$ Pa^{-1}, in comparison with a bulk value of -94×10^{-11} Pa^{-1}. Strain-induced carrier mobility change and surface modifications have been shown to have clear influence on piezoresistance coefficients. This giant piezoresistance effect in Si nanowires may have significant implications in nanowire-based flexible electronics, as well as in nanoelectromechanical systems.

Application of strain to a crystal results in a change in electrical conductivity due to the piezoresistance effect. To evaluate the piezoresistance effect (or electromechanical properties) in nanostructures, mechanical manipulations and electrical measurements must be performed simultaneously. Traditionally, this has been carried out by interfacing the nanostructures with lithographically defined electrodes. Such nanostructure–electrode interfaces[8,10], however, inevitably have stability and reliability issues when subject to mechanical forces. To avoid such interface problems, we have recently developed a chemical vapour deposition process to grow suspended nanowires for piezoresistance testing[11].

Silicon nanowires with ⟨111⟩ or ⟨110⟩ growth directions were grown in trenches on silicon-on-insulator (SOI) wafers to form bridge structures (Fig. 1; Supplementary Information, Fig. S1). Such bridges are themselves monolithically structured and fully functional devices, enabling direct probing of electromechanical properties. The joints between the nanowires and the trench sidewalls are mechanically robust. As shown in Fig. 1b, the nanowire grew backwards after impinging into the opposite wall, implying a self-welding mechanism. The deflection of these nanowires followed exactly the behaviour of double-clamped beams in our atomic force microscopy experiments[12], confirming the rigidity and equivalence of the two joints. The joints also make reliable electrical connections at the nanowire level. Cross-section transmission electron microscopy images show that there is no catalyst metal at either interface (Fig. 1c and e); hence, the wire–wall junctions are simply Si homojunctions with properties determined primarily by carrier distributions. Ohmic behaviour was readily established at the interfaces for the p-type nanowires studied here. The diameters and resistivities of nanowires can be readily controlled. In this study, the nanowires have diameters ranging from 50 to 350 nm and they were made p-type with resistivities of 0.003–10 Ω cm (see Methods).

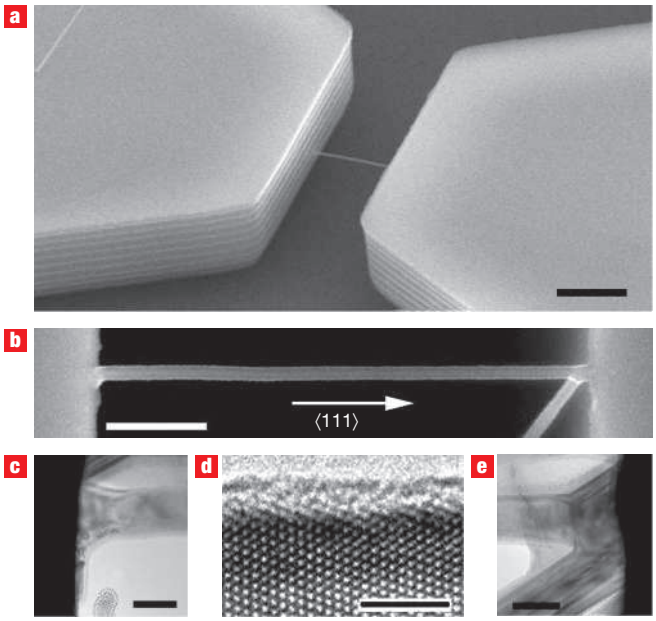

Figure 1 ⟨111⟩-oriented Si nanowire bridges on SOI substrates. a, Single nanowire with the ⟨111⟩ growth direction is bridging a trench confined by vertical {111} faces on a ⟨110⟩-oriented SOI substrate. The parallel lines on the sidewalls with alternating contrast are scallops formed during deep reactive ion etching. **b**, General morphology of a bridged nanowire, which grew from the left sidewall along the ⟨111⟩ direction and impinged upon the opposite sidewall; it finally grew backwards after self-welding into the sidewall. **c,e,** Cross-sectional transmission electron microscope images for the two joints between the nanowire and trench sidewalls. **d**, A high-resolution electron microscopy image confirms the ⟨111⟩ growth direction and reveals a thin oxide layer on the surface of the nanowire. The scale bars in **a**–**e** are 2 μm, 500 nm, 100 nm, 3 nm and 100 nm, respectively.

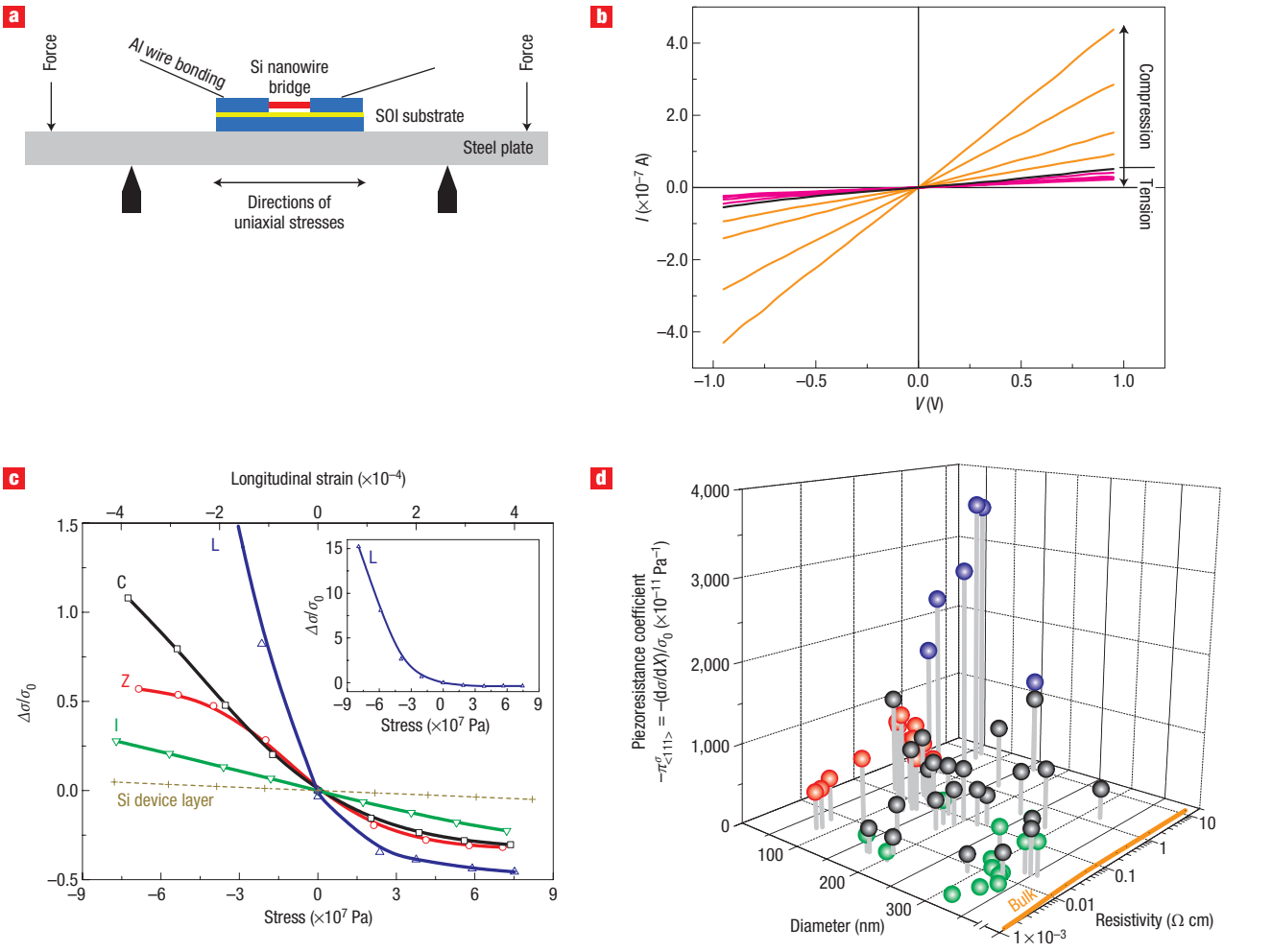

Figure 2 Longitudinal piezoresistance coefficients $\pi^{\sigma}_{\langle 111\rangle}$ of p-type Si nanowires. a, Schematic diagram for the four-point bending setup used to apply uniaxial stresses on Si nanowires. **b**, The conductance of a p-type ⟨111⟩-oriented nanowire (70 nm × 1.2 μm) increases under compressive stresses and decreases under tensile stresses. **c**, Relationships between the relative change in conductivity $\Delta\sigma/\sigma_0$ and stress/longitudinal strain. Four types of nonlinear behaviours of nanowires are shown, labelled with letters I, C, L and Z. The inset shows the overview for L. **d**, First-order longitudinal piezoresistance coefficient of p-type Si nanowires and its dependence on diameter and resistivity. Different colours represent different nonlinearities: green, I; black, C; blue, L; red, Z. The drop lines are for use as guidelines. The uncertainties for $\pi^{\sigma}_{\langle 111\rangle}$ in the fittings are typically 2.5% for I, 2.7% for C, 13.5% for L and 7.8% for Z categories.

The quantitative relation between conductivity/resistivity and stress/strain is given by the fourth-rank piezoresistance tensor[1]. When a uniaxial stress is applied and the electric field and current are along the same direction, the longitudinal piezoresistance coefficient[13] can be measured and defined as the relative change in conductivity per unit stress:

$$\pi_l^{\sigma} = \frac{1}{X}\frac{\Delta\sigma}{\sigma_0}$$

where σ_0 is the conductivity under zero stress and X is the stress. Traditionally, the piezoresistance coefficient was defined with resistivity[1] as $\pi_l^{\rho} = (\Delta\rho/\rho_0)/X$. The conversion is simply $\pi_l^{\rho} = -\pi_l^{\sigma}$ for small $\Delta\sigma$. Uniaxial stresses were applied on Si nanowires along their lengths by the four-point bending method[14] (Fig. 2a; see Methods); the longitudinal piezoresistance coefficients along the ⟨111⟩ and ⟨110⟩ directions, $\pi^{\sigma}_{\langle 111\rangle}$ and $\pi^{\sigma}_{\langle 110\rangle}$, were then examined. The measurements on ⟨111⟩-oriented nanowires will be focused on in the following discussions.

Figure 2b illustrates typical data taken from the four-point bending measurements, showing that the conductance increases under compression and decreases under tension for a p-type ⟨111⟩-oriented nanowire. This trend is qualitatively consistent with the longitudinal piezoresistance behaviour of bulk Si along the ⟨111⟩ directions. For further quantitative analyses, the relative change in conductance $\Delta G/G_0$ was converted to the relative change in conductivity $\Delta\sigma/\sigma_0$ by subtracting the dimensional changes of nanowires (see Supplementary Information). The relationships between $\Delta\sigma/\sigma_0$ and stress X are shown in Fig. 2c. One of the five curves presented is for the boron-doped SOI-device layer, with resistivity 1 Ω cm, as the representative for bulk Si, and the other four curves represent the typical behaviours of Si nanowires. It can be readily seen that the conductivity of a Si nanowire is much more sensitive to stress than that of bulk Si. For instance, under a compression of 8×10^7 Pa, $\Delta\sigma/\sigma_0$ can be as high as 15 for nanowires, but is only 0.08 for bulk Si. Moreover, the

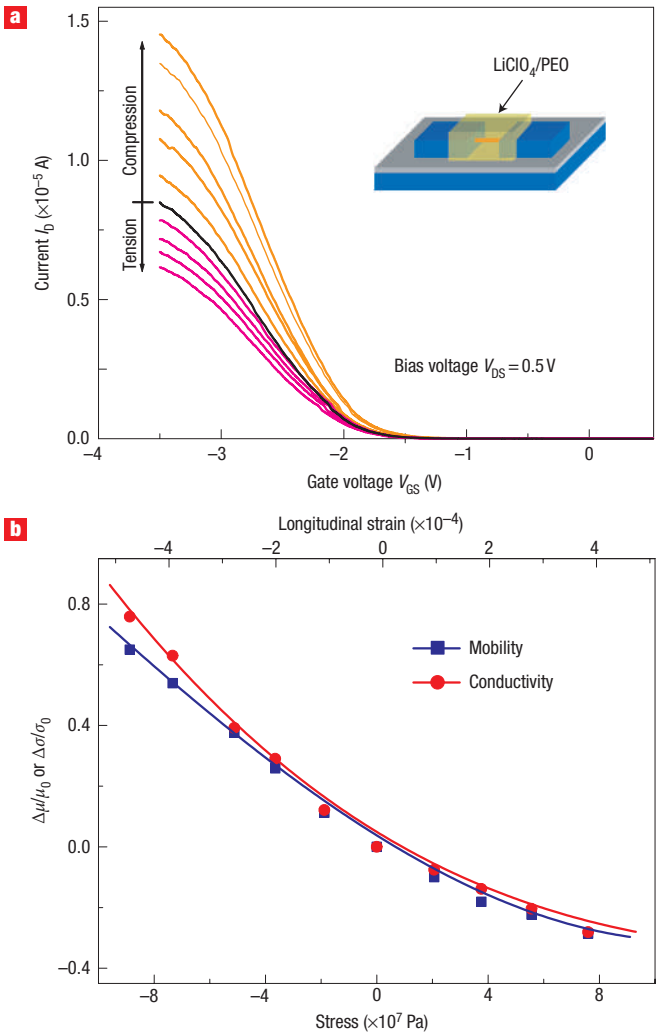

Figure 3 Strained Si nanowire field-effect transistors. a, Measurements on transconductances under different stresses. The inset shows the schematic diagram for polyelectrolyte gating. **b**, Comparison between the relative change in mobility $\Delta\mu/\mu_0$ and the relative change in conductivity $\Delta\sigma/\sigma_0$. The mobilities are fitted and calculated from $V_{GS} = -2.56$ V to -2.9 V and the conductivities are taken at $V_{GS} = -2.74$ V. The nanowire measured here is 120 nm thick and 3.5 μm long.

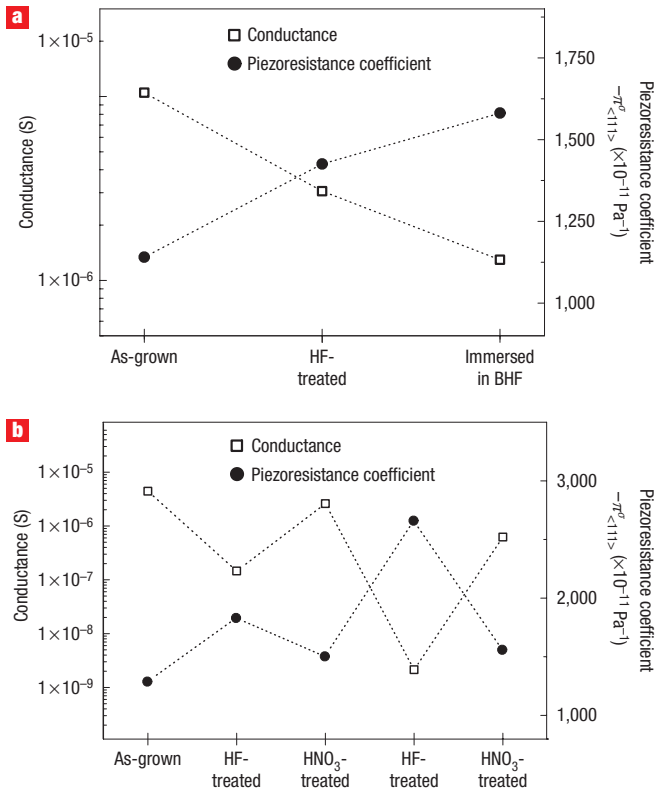

Figure 4 Effects of surface states on the piezoresistance coefficient. The piezoresistance coefficient varies with surface states but remains large. It shows an opposite trend with respect to the conductance during surface treatments. The dotted lines are used as guidelines. **a** and **b** correspond to two different nanowires. The diameters of the nanowires are about 90 nm.

piezoresistance effect is generally nonlinear for Si nanowires, but it is essentially linear for bulk Si (refs 1 and 15) in the stress range performed here. The nonlinearities are classified into four categories based on the shape of the $(\Delta\sigma/\sigma_0)-X$ curves. A letter is assigned to each category by the similarity in shape between the letter and curve: 'I' represents a relatively linear curve, 'C' represents a concave curve, 'L' is for curves with greater slope under compression, and a 'Z' curve is convex with compression and concave with tension. Because of these significant nonlinearities, we fitted $\Delta\sigma/\sigma_0$ as a function of X into the McLaurin series to the third power and took $(d\sigma/dX)/\sigma_0$ at zero stress as the first-order piezoresistance coefficient $\pi^{\sigma}_{\langle 111\rangle}$. The second- and third-order coefficients will not be discussed in detail here; however, it is expected that a large second-order coefficient exists in the C and L curves, and a large third-order coefficient in the Z curves.

Further conclusions can be drawn from the statistical data for $\pi^{\sigma}_{\langle 111\rangle}$ from nanowires with different diameters and resistivities (Fig. 2d; $-\pi^{\sigma}_{\langle 111\rangle}$ was plotted because $\pi^{\sigma}_{\langle 111\rangle}$ is negative). Data for bulk Si with different resistivities[16] are also shown in the figure (carrier concentrations were converted to resistivities by adopting the empirical relation[17]). It is clear that $\pi^{\sigma}_{\langle 111\rangle}$ for a nanowire (-35 to $-3{,}550 \times 10^{-11}$ Pa^{-1}) is generally much higher than that for bulk Si (in the range -17 to -94×10^{-11} Pa^{-1}, depending on resistivities[16]). Only those nanowires with diameters larger than 300 nm and resistivities less than 0.004 Ω cm have values close to that of bulk Si. The resistivity dependence of $\pi^{\sigma}_{\langle 111\rangle}$ for nanowires follows a trend similar to that of bulk: the coefficient increases as the resistivity decreases. In addition, the diameter dependence is particularly interesting: the coefficient increases as the diameter decreases. Furthermore, the nonlinearity of the piezoresistance effect also shows a dependence on diameter and resistivity. From the colour-sorted distribution of the four types of nonlinearities, it can be seen that the nanowires with smaller diameters and higher resistivities have L-shaped $(\Delta\sigma/\sigma_0)-X$ curves, but those with smaller diameters and lower resistivities possess Z curves. Medium-sized nanowires exhibit C shapes, and I curves are quite typical for larger wires with lower resistivities. It is clear that thinner nanowires generally have greater nonlinearities.

For both theoretical considerations and practical applications, it is worth examining whether carrier concentration or mobility plays the dominant role in these remarkable conductivity

changes for nanowires. Strained nanowire field-effect transistors (FETs) were made for such a purpose. Solid polyelectrolyte ($LiClO_4$/poly(ethylene oxide)) was placed over a nanowire to provide surrounding gating[18] and transconductances were measured under varied stresses (Fig. 3a; see Methods). The mobility for the device shown here is estimated to be 30 $cm^2\,V^{-1}\,s^{-1}$ at zero stress and the corresponding carrier concentration is $7 \times 10^{17}\,cm^{-3}$. The relative changes in mobility $\Delta\mu/\mu_0$ were compared with the relative changes in conductivity $\Delta\sigma/\sigma_0$ (Fig. 3b). The close match between them indicates that the large piezoresistance coefficient $\pi^{\sigma}_{\langle 111\rangle}$ derives mainly from the change in carrier mobility. This mobility origin of the giant piezoresistance effect should have significant implications in strain engineering on the nanometre scale. In the current work, the mobility could be doubled for a nanowire with a diameter of 55 nm under 0.05% compressive strain along the ⟨111⟩ direction.

The significant enhancement of the piezoresistance effect is not limited to the ⟨111⟩ direction. Measurements on ⟨110⟩-oriented Si nanowires also show very large longitudinal coefficient $\pi^{\sigma}_{\langle 110\rangle}$ values. For example, $\pi^{\sigma}_{\langle 110\rangle}$ was measured to be $-660 \times 10^{-11}\,Pa^{-1}$ for a 75-nm-thick nanowire with resistivity 0.3 Ω cm (the bulk value for p-type Si is $\pi^{\sigma}_{\langle 110\rangle,bulk} = -70 \times 10^{-11}\,Pa^{-1}$ for the same resistivity[16]). Strained FET experiments also showed the mobility origin for the change in conductance (see Supplementary Information for detailed discussions).

For p-type bulk Si, $\pi_{\langle 111\rangle} \approx \frac{2}{3}\pi_{44}$ and $\pi_{\langle 110\rangle} \approx \pi_{44}/2$, where π_{44} is the shear coefficient. π_{44} originates from the change in mobility through carrier transfers and effective mass changes when the band structures of Si are modified by strains[19]. The mobility origin for $\pi^{\sigma}_{\langle 111\rangle}$ and $\pi^{\sigma}_{\langle 110\rangle}$ in Si nanowires suggests that the enhanced piezoresistance effect will be based on modifications on the band structures. The reduced dimensions and increased surface-to-volume ratio should further contribute to the enhancement.

We note that the slightly enhanced piezoresistance effect has been previously reported in Si beams defined by electron-beam lithography[20]. Some systematic studies on inversion layers of Si metal-oxide-semiconductor devices[21–23] have also been carried out. Several anomalous effects, such as sign reversing from bulk to inversion layers (p-type) for π_{11} and π_{12}, were observed and attributed to the quantization of carriers in the inversion layers. In the case of the nanowires reported here, the quantum confinement simply due to size reduction does not seem evident, given that the diameters of the nanowires are larger than 50 nm. However, the surface effect may contribute significantly here[24]. This surface effect was tested by a series of surface modifications on the suspended nanowires. The as-grown nanowires generally have ~1-nm-thick oxide layers on their surfaces (Fig. 1d). We used HF solution to make the surfaces hydrogen-terminated and used HNO_3 solution to recreate the oxide layers. The conductance of a nanowire was observed to decrease after the treatment with HF or during the immersion in buffered HF; it was brought back by the oxidation in HNO_3 (Fig. 4). The piezoresistance coefficient, however, showed the opposite trend compared with the conductance; that is, it increased after HF treatments and decreased after HNO_3 treatments. These results indicate the importance of surface states in the enhanced piezoresistance effect. Generally, a built-in potential can be readily created near Si surfaces due to Fermi-level pinning at the surface states[25,26], which would mediate the carrier concentrations and induce quantization in the space charge layers[27]. Different surface states have different energy levels and density of states, which would result in different built-in potentials. So, different carrier concentrations and quantization in the space charge layers are expected for different types of surface states. This influence of carrier concentrations on the piezoresistance coefficients has been experimentally demonstrated in the trend shown in Fig. 2d. The possible effect of quantization needs to be simulated in further theoretical work.

We have shown that p-type Si nanowires exhibit unusually large longitudinal piezoresistance coefficients. Systematic theoretical calculations are required to reveal the underlying mechanisms for the observations. The enhanced piezoresistance effect could find applications in Si nanotechnology, flexible electronics[28], as well as in nanoelectromechanical systems. In particular, intrinsic strains may exist in many nanoscale materials[29], and strain sensitivity could be a basic issue affecting the performance of these nanostructure-based electronics.

METHODS

SYNTHESIS OF Si-NANOWIRE BRIDGE STRUCTURES

Si nanowires were grown by using $SiCl_4$ as the precursor in the CVD process. Nanowires with ⟨111⟩ growth directions were synthesized at 850 °C by using Au particles as the catalyst, and nanowires with ⟨110⟩ growth directions were grown at 900 °C by using Pt films as the catalyst. For bridge structures, taking the ⟨111⟩ nanowires as the example, trenches with {111}-face sidewalls were fabricated on ⟨110⟩-oriented SOI wafers. The ⟨111⟩ nanowires would grow perpendicularly to the sidewalls and impinge onto the opposite sidewalls to form suspended bridges (Fig. 1a). In a similar way, ⟨110⟩-nanowire bridges were formed on ⟨111⟩-oriented SOI wafers. The device layer is 5 μm-thick and the buried oxide is 2 μm-thick for all the SOI wafers. Nanowires were doped with boron by using BBr_3 as the source. Single-nanowire-bridged trenches, such as the one shown in Fig. 1a, could be produced at a relatively high yield for single-nanowire-based measurements.

ELECTRICAL MEASUREMENTS

Thin Al wires were directly bonded onto Si pads by ultrasonic power to complete the connections for electric measurements. The contacts are ohmic and have resistances of ~100 Ω. The SOI device layer was doped with boron with a resistivity of 0.01 Ω cm, and the Si pads coupled with trenches have resistances of ~50 Ω. These two resistances are only 0.001 to 0.1% of the resistance of a Si nanowire and can be neglected in the measurements. Four terminal electrical measurements were applied for SOI device layers.

FOUR-POINT BENDING METHOD

The SOI substrate with Si-nanowire bridges, together with a control bare SOI substrate side-by-side, was adhered firmly onto a 1.2-mm-thick steel plate using epoxy. Both substrates were aligned to have their device ⟨111⟩/⟨110⟩ directions parallel to the longitudinal direction of the steel plate. When the plate was subject to four-point bending (Fig. 2a), uniaxial stresses were created longitudinally in the pure bending region (between the two inner supports)[30]. Any transverse stresses (estimated to be 10% of the longitudinal stresses), which could be generated in the Si substrates due to the difference in Poisson's ratio between the steel and Si, will not be transferred to the Si nanowires, because the nanowires are suspended with only the two ends mechanically anchored to the Si substrate[20]. The non-uniformity of stresses was found to be only ~0.01% across the nanowire's diameter, which was determined by the ratio of the diameter to the distance from it to the plate's neutral axis. So, nanowires are believed to be subjected to uniaxial stresses to a very accurate degree in four-point bending experiments. Tensile stresses were generated on the nanowires in the bending direction shown in Fig. 2a, and compressive stresses were obtained by reversing the bending direction. It was ensured that the compressive stresses applied were less than the critical stresses to prevent the nanowires from buckling (see Supplementary Information). A foil strain gauge was glued on the surface of the control substrate to measure the longitudinal strains, which were converted to stresses by multiplying by Young's modulus (Young's modulus for nanowires is similar to that of bulk[12]). The strains measured by the foil gauge were checked to ensure consistency with the deflections of the plate. Measurements on SOI-device layers gave approximate values (with about +5% error) of $\pi^{\sigma}_{\langle 111\rangle}$ due to the existence of transverse stresses; they were used as the bulk references to check the consistency of the experiments. $\pi^{\sigma}_{\langle 111\rangle}$ measured from device layers was close to the value of bulk Si; for example, $\pi^{\sigma}_{\langle 111\rangle} \approx -80 \times 10^{-11}\,Pa^{-1}$ for a device layer with resistivity of 1 Ω cm. $\pi^{\sigma}_{\langle 111\rangle}$ was also checked for the device layer (0.01 Ω cm) on every sample, with consistent values of $-57 \pm 5 \times 10^{-11}\,Pa^{-1}$.

POLYELECTROLYTE GATING

An extra Al wire was bonded on the SOI oxide surface near the nanowire as the gating electrode. $LiClO_4$ and poly(ethylene oxide) were mixed by weight ratio 0.15:1 in methanol and briefly heated at 80 °C to form a gel-like polyelectrolyte. The polyelectrolyte was placed over the nanowire and the Al wire to provide surrounding gating via the electric double layer established at the nanowire–polyelectrolyte interface. The mobilities were calculated from the slopes of the linear region in the transfer characteristics, in which the capacitance from the native oxide layer on the nanowire was considered. The polyelectrolyte was considerably soft and expected to have negligible influence on the mechanical behaviour of the nanowires.

CHEMICAL MODIFICATIONS OF Si NANOWIRE SURFACES

5% HF solution or 10:1 (NH_4F/HF) buffered HF solution (for immersion) was used to provide hydrogen termination and 70% HNO_3 was used to oxidize the surfaces. All the treatments took 30 s except for the immersion experiments.

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Competing financial interests

The authors declare that they have no competing financial interests.