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Growth and Electrical Characteristics of Platinum-Nanoparticle-Catalyzed Silicon Nanowires**

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Silicon nanowires (Si NWs) will likely revolutionize a wide variety of applications ranging from field-effect transistors[1–4] (FETs) and other nanoelectronics to chemical and biological sensing,[5] and even solar cells.[6,7] These nanowire devices must be integrated with more traditional electronic or optical components to make a complete usable system, which will probably require standard silicon clean-room processing. Nearly all Si NWs are made using a gold (or gold-based) catalyst and the well-known vapor–liquid–solid (VLS) growth mechanism first discovered by Wagner and Ellis.[7,8] Because Au creates mid-gap trap states in silicon, it poisons device performance and typically is not allowed for use in electronics-fabrication labs and clean rooms.[9] Therefore a new, electronics-friendly catalyst is critical not only for nanowire electronics, but also for integrated devices incorporating Si NWs in any capacity. Several groups have successfully grown Si NWs with alternative catalyst thin films such as Ti,[10] Al,[11] Pt,[12] and PtSi[13] but extensive electrical characterization that is very important for many device applications has not been conducted. In this report, Pt was chosen as a catalyst because it has a high melting point, can be made into nanoparticles with a tight size distribution and shows orders-of-magnitude-lower leakage current when incorporated into silicon diodes compared to gold.[9,14,15] We have developed a chemical-vapor-deposition (CVD) synthesis based on our previous experience with gold catalysts[16] to grow high-quality single-crystalline size-controlled epitaxial Si NWs from various sized Pt nanoparticles. The nanowires were characterized by using scanning electron microscopy (SEM) and transmission electron microscopy (TEM) to determine their size distribution, growth direction, and alignment, whereas their electrical properties were tested by making planar FETs.

Unlike the Au–Si system, Pt does not form a simple eutectic with Si; rather, there are several stable platinum silicide compounds in the 800–1000 °C temperature range where Si-NW growth occurs.[17] There is a eutectic formed between PtSi and Si at 979 °C, so at temperatures above this point and at high Si concentrations, it is thermodynamically favorable to precipitate pure Si.[17,18] Si-NW growth below 979 °C can be explained by two possible mechanisms. First, because the Pt nanoparticles begin melting (at least surface melting) around 600 °C,[19,20] which is about 1000 °C lower than the bulk melting point, the bulk phase diagram may not accurately represent the phase transitions occurring in the catalyst nanoparticle tip. In a very simplistic view, all the phase boundaries should shift down in temperature, with the Pt-rich phases being affected more strongly than the Si-rich phases. With a shift of over 1000 °C at the pure platinum side of the phase diagram, a 180 °C shift for the PtSi–Si eutectic down to 799 °C at 67 % Si seems likely. Several reports also show that Pt nanoparticles annealed in a hydrogen atmosphere at temperatures as low as 600 °C on silica substrates form Pt_xSi_y.[21,22] Additionally, Wagner and Ellis found that even Pt thin films as thick as 100 nm on Si formed a liquid surface layer at temperatures as low as 850 °C, further supporting a significant temperature decrease of the PtSi eutectic point from the bulk value.[23]

The second possible explanation is that the Pt nanoparticles do not completely melt and instead act as an active site for rapid $SiCl_4$ decomposition and diffusion, leading to a vapor–solid–solid (VSS) rather than VLS growth mechanism. The VSS mechanism has been proposed to explain the growth of several other semiconducting nanowires, particularly III–V compounds, that were originally thought to grow according to the VLS mechanism.[24,25] In a recent report, Pt thin films deposited on Si were annealed at 800 °C in a hydrogen atmosphere to form PtSi islands which in turn were used to catalyze Si-NW growth at temperatures between 500 and 700 °C through a proposed VSS mechanism.[13] Considering the strong in situ TEM evidence from the literature mentioned above that the Pt nanoparticles begin melting well below their reaction temperatures, the island formation observed for Pt/Si films near 800 °C, and the evidence of strong eutectic-point depression seen for Pt thin films on Si, the Si NWs in this study most likely grow via the VLS mechanism. However, the VSS mechanism cannot be ruled out without in situ TEM evidence.

Pt nanoparticle catalysts with average diameters of (9.3 ± 1.2) nm were used to synthesize Si NWs with average diameters of (11.3 ± 1.6) nm (Fig. 1). The standard deviations of the starting colloid and the resulting wire diameters were

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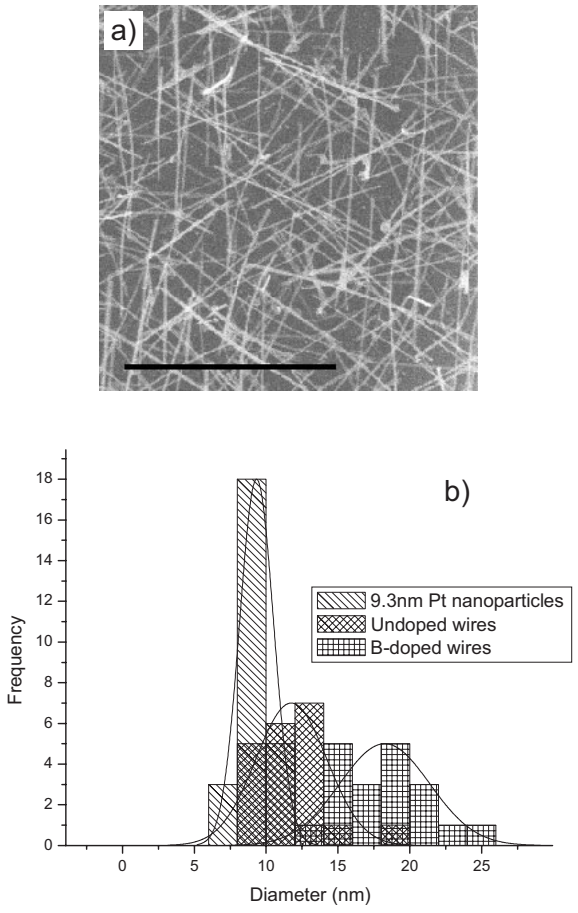

Figure 1. a) SEM images of boron-doped Si NWs grown from 9.3 nm Pt nanoparticles on a single-crystalline Si (111) substrate. The scale bar is 1 μm. b) Size distribution of the 9.3 nm Pt catalyst particles and the resulting undoped and boron-doped Si NWs.

essentially the same, whereas the wires were 22 % larger than the particles. This one-to-one catalyst-to-wire growth has been demonstrated many times with gold catalysts in various semiconductor systems including Si, Ge, ZnO, and many III–V compounds.[7,16,26–29] The increased average size has previously been explained in the Au–Si system by droplet swelling during Si incorporation and eutectic formation in the initial step of VLS growth.[26,30]

The size distribution was taken by measuring the wire diameters near the tip for every sample because the wire diameter at the base depends strongly on reaction conditions; tapering can be tuned by controlling the rate of uncatalyzed thin-film deposition on the wire sidewalls. The hydrogen reduction of $SiCl_4$ is highly endothermic and thus becomes more favorable at high temperatures.[31] For this reason, to avoid tapering from sidewall deposition it is important to maintain the lowest possible temperature while still allowing the reaction to proceed. Lower partial pressures of $SiCl_4$ and total gas flow rates reduced thin-film deposition as well. Boron doping is also known to promote $SiCl_4$ decomposition, adding another complicating factor for optimizing growth conditions in doped wires.[31] In fact, boron-doped wires typically had a larger diameter of about (17.9 ± 3.1) nm but otherwise were very similar to the undoped wires (Fig. 1). The increased diameter may be due to higher supersaturation or boron incorporation in the droplet. Additionally, turning the growth substrate upside down on the reaction plate led to completely untapered Si NWs; the diameter increased less than 1 nm from the tip to several microns along the wire. This deposition scheme presumably works by hindering gas diffusion and leading to locally elevated product (HCl) concentrations and reduced reactant ($SiCl_4$) concentrations around the nanowires. It is well-known that silicon thin-film deposition rates can be controlled by tuning the ratio of HCl to $SiCl_4$ and Sharma et al. showed that adding HCl to the SiH_4 reactant stream reduced tapering dramatically.[10]

According to the TEM imaging, all the wires were single crystalline and nearly all were free from defects such as dislocations or twinning planes (Fig. 2). The catalyst tip was always round and while the interface with the wire was not atomically sharp it was generally perpendicular to the growth direction. According to the electron diffraction patterns, the nanowires grew predominantly in the <110> direction regardless of the amount of tapering, although <111>, <310>, <311>, and <210>-oriented wires also appeared (Fig. 2). The propensity for the <110> growth direction in these wires is similar to results from previous studies of small-diameter Au catalyzed Si NWs.[30,32] In the Au–Si case, the growth direction changes from <111> to <210> and then <110> as wire diameters go from greater than 30 to less than 10 nm. Wu et al. attributed the crossover to surface-energy considerations; at smaller diameters, surface energy becomes very important so <110> oriented wires that allow for lower-energy {111} side facets replace <111> oriented wires that have higher-energy {110} facets. Pt-catalyst particles larger than 9.3 nm were not available, but Si NWs larger than 30 nm in diameter grown from Pt thin films did continue to show a preferred <110> orientation, suggesting that the growth direction may depend not only on the size, but also on the catalyst.[33] This is reasonable considering Pt and Au have different surface energies and eutectic compositions. However, Wagner and Ellis found that silicon whiskers close to 10 μm in diameter catalyzed by Pt thin films grew in the <111> direction,[23] so Pt may simply shift the growth-direction transition point.

Because the wires grow primarily in the <110> direction, vertically aligned wires can be obtained on Si {110} wafers. This concept has been demonstrated previously in the Au–Si system on Si {111} wafers where the wires grow primarily in the <111> direction.[16,27] Vertical alignment can be controlled by adjusting the reaction conditions, but as noted by Hochbaum et al.,[16] 100 % vertical alignment is difficult to achieve with very small catalyst particles. Figure 3a shows a cross-sectional SEM image of a sample showing good epitaxy and moderate vertical alignment viewed from one of the four equivalent {111} directions. Several off-vertical <110>-oriented Si NWs are clearly visible in addition to some nonepitaxial wires that are due mainly to clumping and damage during wafer cleaving.

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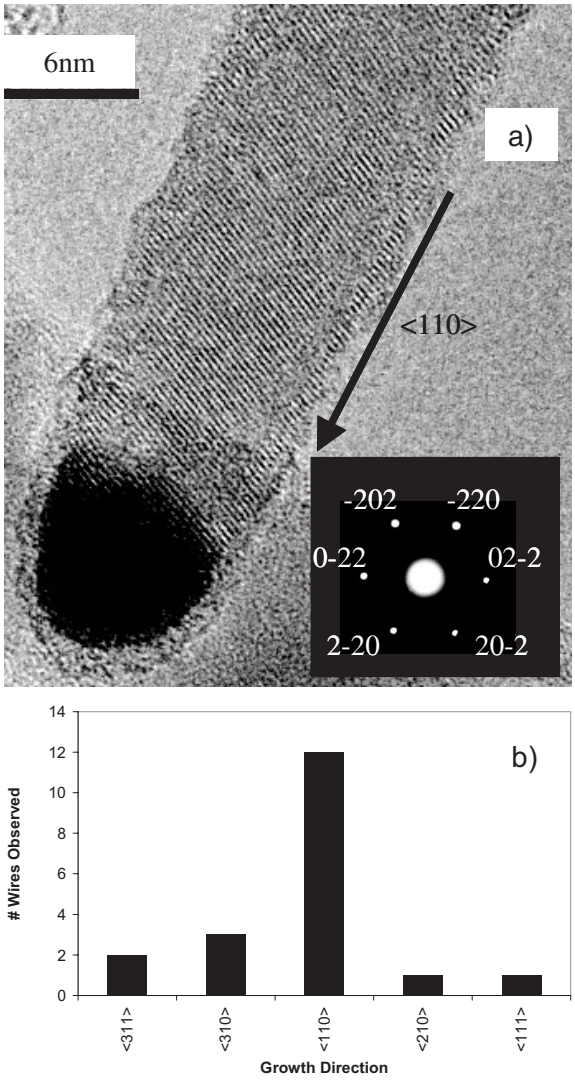

Figure 2. a) Lattice-resolved phase-contrast TEM image and corresponding diffraction pattern taken along the [111] zone axis showing a defect-free single-crystalline Si NW and the Pt (or PtSi) catalyst tip. b) A histogram showing the dominant <110> growth direction observed for the Pt catalyzed Si NWs.

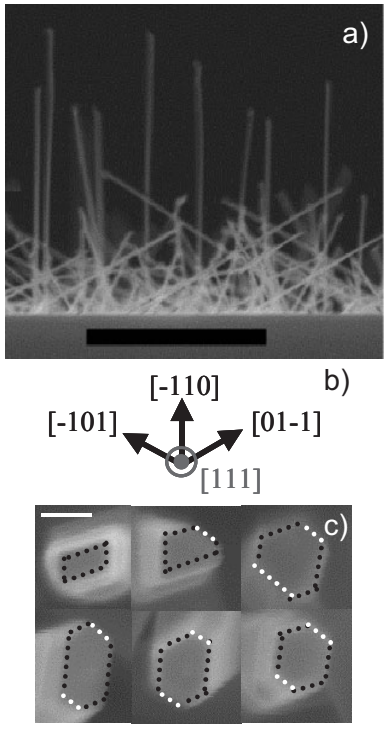

Figure 3. SEM images of vertically aligned Pt nanoparticle catalyzed Si NWs grown on Si {110} substrates. a) Untapered wires viewed in cross section from the [111] direction showing some vertical alignment and off-vertical epitaxial wires. The scale bar is 1 μm. b) Diagram showing the angles expected for epitaxial <110>-oriented Si NWs viewed from the [111] direction. c) Top view of wires grown under conditions promoting thin-film deposition leading to thicker wires where {111} (black) and {100} (white) faceting can be identified from the wafer cleavage planes. The scale bar is 50 nm.

The vertically aligned Si NWs in this report provide a unique opportunity to observe the cross-sectional shape and sidewall faceting of <110>-oriented wires using SEM. This technique provides several advantages over cross-sectional TEM for determining nanowire capping planes. First, there is no required sample preparation. The cross-sectional TEM technique requires extensive post-growth processing including wire alignment, oxide encapsulation, and sample thinning.[30,34] As a direct consequence, it is difficult to examine a large number of wire cross sections with TEM, while this is easy in SEM. Second, cross-sectional TEM requires very careful alignment to ensure that the interface being examined is truly normal to the wire length. However, in plan view SEM pictures, vertical wires will all be perpendicular to the growth axis (within a few degrees) and the crystallographic directions are clear from the off-vertical epitaxial wires or the cleavage planes of the single-crystalline silicon substrate. However, SEM resolution limits require the wires be at least 30 nm in diameter in order to resolve faceting. For this reason, Pt-catalyzed Si NWs were grown under conditions that promoted rapid thin-film deposition to increase the wire diameter. Figure 3C shows the shapes observed in plan-view SEM pictures and identifies the terminating crystal faces. Because silicon wafers prefer to cleave along the low-surface-energy {111} planes, the crystallographic directions can be determined simply from the shape of the fractured wafer. In fact, all samples showed the rhobohedral shape expected from a {110} wafer with {111} side planes. Figure 3c clearly shows that the four {111} faces dominate all cross-sectional shapes, but 80 % of the wires also include two {100} faces with a wide variety of length ratios. Hexagonal-shaped wires with four {111} and two {100} planes have been observed in previous cross-sectional TEM studies.[30,34] Quadrilateral and pentagonal cross sections seen here have not been reported in <110>-oriented Si NWs although they have been theoretically predicted to be stable.[35] In fact, it was recently shown that for very small Si NWs (near 1–2 nm diameter) oriented along <110> and passivated with hydrogen, quadrilateral and hexagonal cross

sections should have nearly the same stability.[36] As the wire diameter increases beyond 2 nm, hexagonal shapes become slightly more stable but the transition is not well defined. The current experimental results agree very well with the theoretical predictions: because the hexagonal wires are more stable, they dominate, whereas the quadrilateral wires still rarely appear and the pentagonal wires provide an intermediate between the quadrilateral and hexagonal shapes. The wide range of side ratios in the hexagonal wires also supports a transition between shapes, where subtle differences in sidewall deposition rates on the equivalent {111} faces leads to distinct shapes.

The major motivation to replace gold with an alternative catalyst is to make Si-NW growth compatible with micro- and nanofabrication. Therefore, it is important to test the electrical properties of any new catalyst system to ensure that it will allow for reasonable device performance. To this end, fifteen planar FETs were fabricated from boron-doped Si NWs to measure their electrical properties. Figure 4 shows an SEM image and the current–voltage (*I–V*) and transfer characteristics of our best device. The *I–V* plot is linear and the drain–source current (I_{ds}) varies dramatically with gate voltage (V_g). The gate effect is especially pronounced in the region between $V_g = 0$ and $V_g = -2.5$, where the Si-NW FET turns on and I_{ds} increases from 0 to around 100 nA. The mobility extracted from the transconductance slope is 28 $cm^2 V^{-1}s^{-1}$, whereas the on/off ratio determined from a log plot of the transfer characteristics is 7400. The remainder of the wires measured also showed linear or nearly linear *I–V* curves, although most of them needed a small negative gate bias between –0.5 and –5 V to show any current. This phenomenon suggests that there are trapped charge states on the surface that act as an artificial gate. The effect is greatly enhanced because of the small NW diameter and high surface-to-volume ratio. Even at a slow gate voltage scan rate (50 $mV s^{-1}$), the I_{ds}-versus-V_g plots typically showed a 0.5–1 V hysteresis between the forward and reverse scans providing further evidence of trapped surface charge. In the on state the wires had resistances in the megaohm range leading to resistivities between 0.1 and 140 Ωcm. Mobility and on/off ratio values varied from 0.04 to 28 $cm^2 V^{-1}s^{-1}$ and 480 to 7400, respectively, which are in the same range as those previously reported for unfunctionalized Au-catalyzed Si NWs.[1,3,37,38]

In conclusion, we have demonstrated that platinum nanoparticles offer a viable alternative to the traditional gold catalyst for gas-phase CVD synthesis of single-crystalline size-controlled epitaxial Si NWs for nanoelectronics applications. Undoped wires grown from 9.3 nm Pt nanoparticles had average diameters of 11.3 nm, whereas boron-doped wires were larger at 17.9 nm. The Si NWs grew predominantly in the <110> direction, leading to partially vertically aligned Si NWs on single-crystalline Si {110} wafers. Despite strong surface effects stemming from the small diameters, the electrical properties of boron-doped wires were comparable to other unfunctionalized Si-NW FETs with the best mobility and on/off ratio being 28 $cm^2 V^{-1}s^{-1}$, and 7400, respectively. In addition to reducing the microelectronics-processing concerns related to gold, the Pt catalyst allows 9 nm particles to be used in high temperature $SiCl_4$-CVD reactors without significant aggregation. This simultaneously allows for small-diameter wires and facile integration.

Experimental

The Pt nanoparticles were synthesized by procedures developed in our group [14]. Hexachloroplatinic acid was reduced by ethylene glycol at reflux in the presence of polyvinylpyrrolidone (PVP). The particles were precipitated in acetone and washed thoroughly with ethanol before being dispersed in water. The approximate concentration of the stock solution was roughly 10^{15} particles cm^{-3} and this stock solution was diluted in either water or isopropyl alcohol (IPA) for Pt-nanoparticle deposition on the silicon substrate according to the desired wire density.

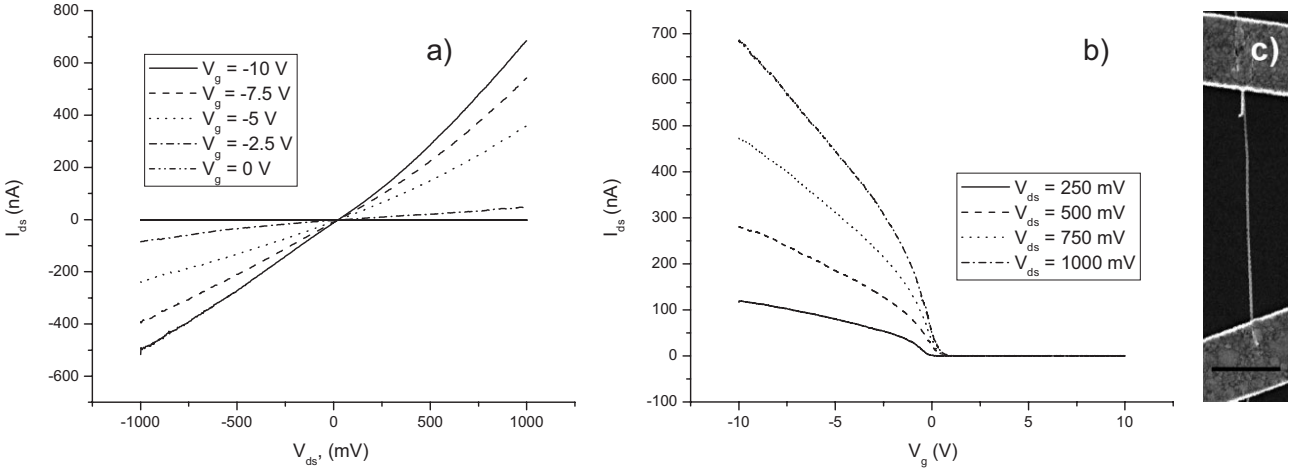

Figure 4. Electrical properties of a boron-doped Pt-nanoparticle catalyzed Si NWs. a) Drain–source current (I_{ds}) plotted versus drain–source voltage (V_{ds}) at gate voltages (V_g) of –10, –7.5, –5, –2.5, and 0 V. b) Transfer characteristics of the same device at $V_{ds} = 250$, 500, 750, and 1000 mV. c) SEM of the Si-NW FET top-contacted by drain and source electrodes. The scale bar is 1 μm.

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Silicon wafers (Montco Silicon Technologies) with various orientations, doping levels, and carrier types were cleaved using a diamond scribe into pieces approximately 5 mm on a side and cleaned by sonicating in acetone then IPA for several minutes each and blown dry with nitrogen. Then they were treated in a solution of 10 parts ammonium fluoride to 1 part hydrofluoric acid (10:1 BHF) to remove the native oxide layer. Typically, 30 μL of Pt nanoparticle solution were drop-cast on the silicon surface and after 20 s this was rinsed with IPA and blown dry in nitrogen. Si NWs were grown in a home-built atmospheric-pressure CVD system for 2–30 min at 805 °C, 50 standard cubic centimeters per minute (sccm) of carrier gas (10 % H_2/Ar) and 7.5 sccm of carrier gas bubbled through liquid silicon tetrachloride ($SiCl_4$). The growth rate was approximately 300 nm min^{-1}. Boron trichloride (BCl_3) gas was used for the boron-doped Si NWs with a typical flow rate of 0.5 sccm.

SEM images were taken with a JEOL 6340F or FEI Strata 235. Size-distribution data was collected on a JEOL 200CX transmission electron microscope, while growth directions, diffraction patterns, and phase-contrast images were collected on a Philips CM200/FEG transmission electron microscope.

Planar FETs were fabricated using boron-doped wires and standard electron-beam lithography on a JEOL 6400 scanning electron microscope and Nanometer Pattern Generation System (NPGS). The nanowires were sonicated off the substrate in VLSI-grade IPA and drop-cast on a chip containing prepatterned metal electrodes on 600 nm of thermal silicon oxide and 50 nm of silicon nitride covering an n-Si (Sb-doped) chip with a resistivity of 0.008 Ωcm. The area underneath the wires only contained the 50 nm silicon nitride dielectric (a small window of oxide had previously been removed) to improve gate coupling without increasing leakage current. After writing the electron-beam pattern and developing in methyl isobutyl ketone (MIBK) the native oxide was removed using 10:1 BHF. The substrate was immediately loaded into a high vacuum chamber to deposit electron-beam-evaporated Ti/Au (100 nm/100 nm) as the contact metal. Then it was annealed in forming gas (10 % H_2/N_2) at 300 °C for 3 min to reduce the contact resistance and give ohmic contacts. Electrical measurements were made on a home-built probe station using a National Instruments PCI-6052E and Keithley 428 current amplifier controlled by a Labview program. The conductivity, mobility, and on/off ratio were extracted from the current-voltage and transfer characteristic plots using standard equations [1,38].

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