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Synthesis and Thermoelectrical Characterization of Lead Chalcogenide Nanowires**

By *Melissa Fardy*, *Allon I. Hochbaum*, *Joshua Goldberger*, *Minjuan M. Zhang*, and *Peidong Yang**

Thermoelectricity is the phenomenon of conversion between thermal and electrical energy. Compared with other technologies, thermoelectric (TE) devices offer distinct advantages: they have no moving parts, contain no chlorofluorocarbons, and have a long lifetime of reliable operation. However, current TE materials have found limited commercial application due to their low efficiency. TE efficiency is related to a material-dependent coefficient, Z, and is often expressed as the dimensionless figure-of-merit, ZT, given by $ZT = \sigma S^2 T/\kappa$, where T is the absolute temperature, σ is the electrical conductivity, S is the Seebeck coefficient, and κ is the total thermal conductivity. It becomes difficult to improve ZT beyond a certain point since the material properties S, σ, and κ are inter-dependent.[1] Presently, simple bulk materials have reached an upper limit of ZT at approximately 1. Hicks and Dresselhaus proposed that conversion of bulk materials to low dimensional materials might significantly enhance TE performance through phonon scattering and electron confinement effects.[2] Dimensional reduction has since been shown to increase boundary scattering of phonons and reduce lattice thermal conductivity,[3] possibly without negatively affecting the electrical conductivity or Seebeck coefficient. The positive effects of low-dimensionality on ZT have already been demonstrated through several theoretical[2,4–6] and experimental[7] investigations, a few of which were based on lead chalcogenide systems.[8,9] Harman et al. achieved an especially high ZT of 2.0 at 300 K with PbSeTe/PbTe quantum dot superlattices.[10] Bulk PbS, PbSe, and PbTe possess a relatively high ZT, so synthesizing these materials as one-dimensional structures is a promising method for further improvement in the figure-of-merit.

A variety of methods have been utilized to synthesize PbX (X = S, Se, Te) nanowires, including templating in mesoporous silica channels,[11] oriented attachment of nanoparticles,[12] seeded solution synthesis,[13] colloidal synthesis,[14] and solvothermal,[15] hydrothermal,[16] and soft template routes.[17] A facile chemical vapor transport (CVT) synthesis of thin, high-aspect ratio PbS nanowire arrays has also been reported.[18] This last method produces high-quality, single crystalline nanowires, highlighting CVT as a promising method for synthesis of PbX nanowires as novel TE materials.

Here we report the CVT synthesis of arrays of PbS, PbSe, and PbTe nanowires and the characterization of their thermal and electrical properties to investigate their potential as TE materials. All nanowires were prepared by chemical vapor transport of Pb and chalcogen precursors inside a horizontal tube furnace. Alumina boats filled with $PbCl_2$ and the desired chalcogen were positioned in a quartz tube near the center of the furnace. Si (100) substrates were placed downstream from the precursors in the cooler region of the tube to collect the deposited products. In each synthesis, the furnace was heated to the reaction temperature for 10 minutes under a carrier gas flow of N_2, 5 % H_2 balance N_2, Ar, or 10 % H_2 balance Ar.

X-ray diffraction (XRD) patterns (Fig. 1) taken from the as-synthesized nanowire substrates demonstrate the high quality, crystalline nature of the materials. Substrates chosen

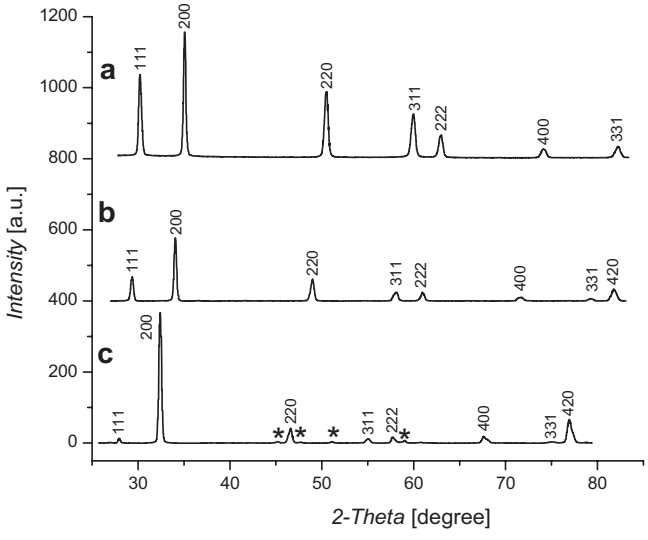

Figure 1. XRD patterns taken from a) PbS, b) PbSe, and c) PbTe nanowire substrates (stars indicate Te peaks), which confirm their chemical composition and fcc structure.

[*] Prof. P. Yang, M. Fardy, A. I. Hochbaum, Dr. J. Goldberger
Department of Chemistry, University of California, Berkeley
Berkeley, CA 94720 (USA)
E-mail: p_yang@berkeley.edu
Prof. P. Yang, M. Fardy, A. I. Hochbaum, Dr. J. Goldberger
Materials Sciences Division, Lawrence Berkeley National Laboratory
1 Cyclotron Road, Berkeley, CA 94720 (USA)
Dr. M. M. Zhang
Materials Research Department, Toyota Technical Center, Toyota Motor Engineering & Manufacturing North America (TEMA) Inc.
2350 Green Road, Ann Arbor, MI 48105 (USA)

[**] M. F. and A. I. H. contributed equally to this work. We thank Renkun Chen for helpful discussion and assistance with thermal characterization. A. I. H. thanks the National Science Foundation for an IGERT graduate research fellowship. We thank the National Center for Electron Microscopy and the UC Berkeley Microfabrication Laboratory for the use of their facilities.

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for XRD characterization were covered with nanowires over an area of 1–3 cm^2. The diffraction peaks in each pattern were indexed to face-centered-cubic (fcc) structures of pure PbS, PbSe, and PbTe, with calculated lattice constants of 5.943 Å, 6.116 Å, and 6.406 Å, respectively. These lattice constants correspond well to those of the bulk material, 5.94 Å (PbS), 6.12 Å (PbSe), and 6.50 Å (PbTe).[19] The minor peaks in the PbTe pattern belong to hexagonal Te. This Te was likely deposited as particulates or thin film, but was not present on the nanowire surfaces, as confirmed by transmission electron microscopy (TEM) imaging.

The morphologies of the PbX nanowires were examined using both scanning electron microscopy (SEM) and TEM. The nanowires grown in this CVT synthesis have similar diameter and length distributions, independent of the material. The typical diameters and lengths of the nanowires are 40–100 nm and 10–70 μm for PbS (Fig. 2a and b), 40–200 nm and 10–100 μm for PbSe (Fig. 2c and d), and 100–200 nm and 40–100 μm for PbTe (Fig. 2e and f). As shown in the SEM images in Figure 2, the nanowires in each array are aligned either parallel or perpendicular to one another and are arranged in two different types of arrays. The first type of array (Fig. 2, left column) has been previously reported for PbS CVT nanowires and consists of a central cube with nanowires growing perpendicularly from each of the six faces.[18] In this case, Ge et al. proposed a homogeneous, epitaxial growth process in which defects on the surfaces of the cubes serve as nucleation sites for the nanowire growth. The second type of array is self-supporting and does not contain a central cube (Fig. 2, right column).[20] The morphology of these arrays varies between a net of wires and a structure similar to that of the orthogonal arrays with cubes. The nucleation and growth mechanism of these arrays is unknown at this time and will require further investigation.

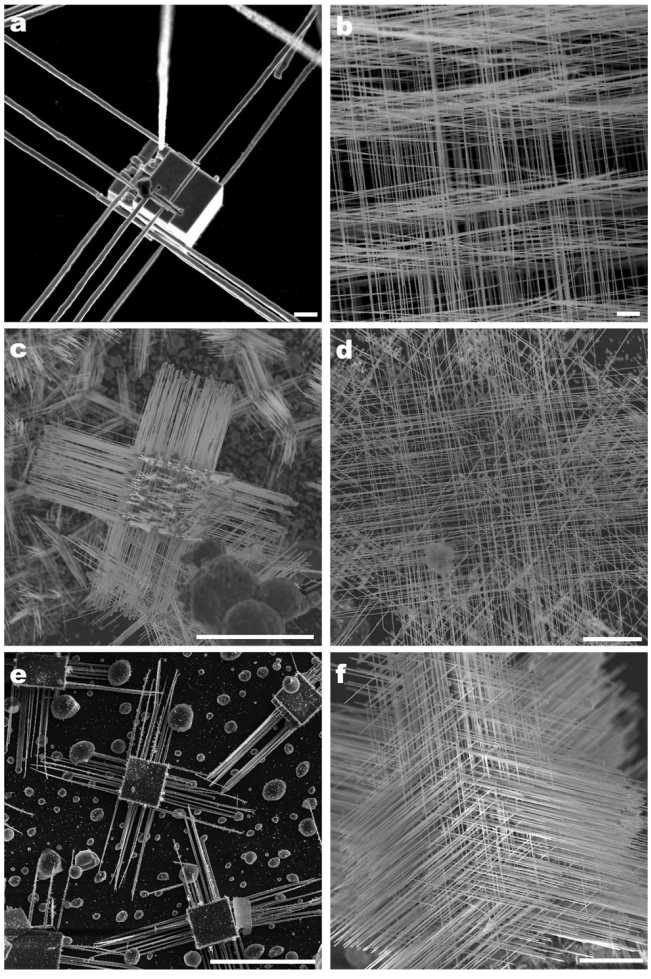

Figure 2. SEM images displaying central cube arrays (left column) and self-supporting arrays (right column) of a) and b) PbS nanowires, scale bars are 1 μm, c) and d) PbSe nanowires, scale bars are 10 μm, and e) and f) PbTe nanowires, scales bar are 50 μm and 10 μm, respectively.

The selected area electron diffraction (SAED) patterns (Fig. 3a–c, insets), taken from the [100] zone axis, suggest that the nanowires are single crystalline and grow along the <100> directions. No secondary or hexagonal phases were detected, thus confirming that the crystalline Te observed in the XRD pattern was not deposited on the nanowires. The single crystallinity and structural parameters were further verified by high-resolution transmission electron microscopy (HRTEM) images of the nanowires (Fig. 3a–c). The energy-dispersive X-ray (EDX) spectra (Fig. 3d–3f) also confirm their purity, with the Cu peaks arising from the copper grids used for TEM analysis. Cl peaks were also detected and likely result from surface impurities remaining from the $PbCl_2$ precursor. In addition to the aforementioned species, the EDX spectra show presence of both Si and O signals. As seen in the HRTEM images, the nanowires have 2–6 nm amorphous silica coatings. This silica coating can be etched using buffered hydrofluoric acid (BHF) solution. Several groups have previously reported amorphous silica coatings on CVT-synthesized PbS nanowires.[18,20] This silica most likely originates from etching of the silicon substrates and quartz reaction tube during the synthetic process.[21]

Electronic properties of CVT-grown PbX nanowires were measured using contacts patterned by electron-beam lithography (EBL). Nanowires were sonicated into isopropanol, and the suspension was drop-cast onto prefabricated substrates. The substrates were then soaked in 10:1 BHF to selectively remove the insulating silica coating on the outer surface of the nanowires. For the cases of PbS and PbTe, little to no degradation or measurable contraction of the nanowire diameter was observed in HRTEM after the samples were treated with BHF. However, the outer amorphous silica shell can be completely removed. The PbSe nanowires, on the other hand, were etched away completely after 20–30 seconds BHF exposure. Instead, PbSe nanowires were contacted by local Pt deposition in a focused ion beam microscope on the thermal measurement devices. Figure 4a shows the *I–V* characteristics for a 63 nm diameter PbS nanowire field-effect transistor (FET) device under different gate voltages. The device is p-type with a resistivity of 1.7 Ω cm. The calculated carrier concentration is 3.7×10^{18} cm^{-3} and the mobility is 1.0 $cm^2\,V^{-1}\,s^{-1}$,

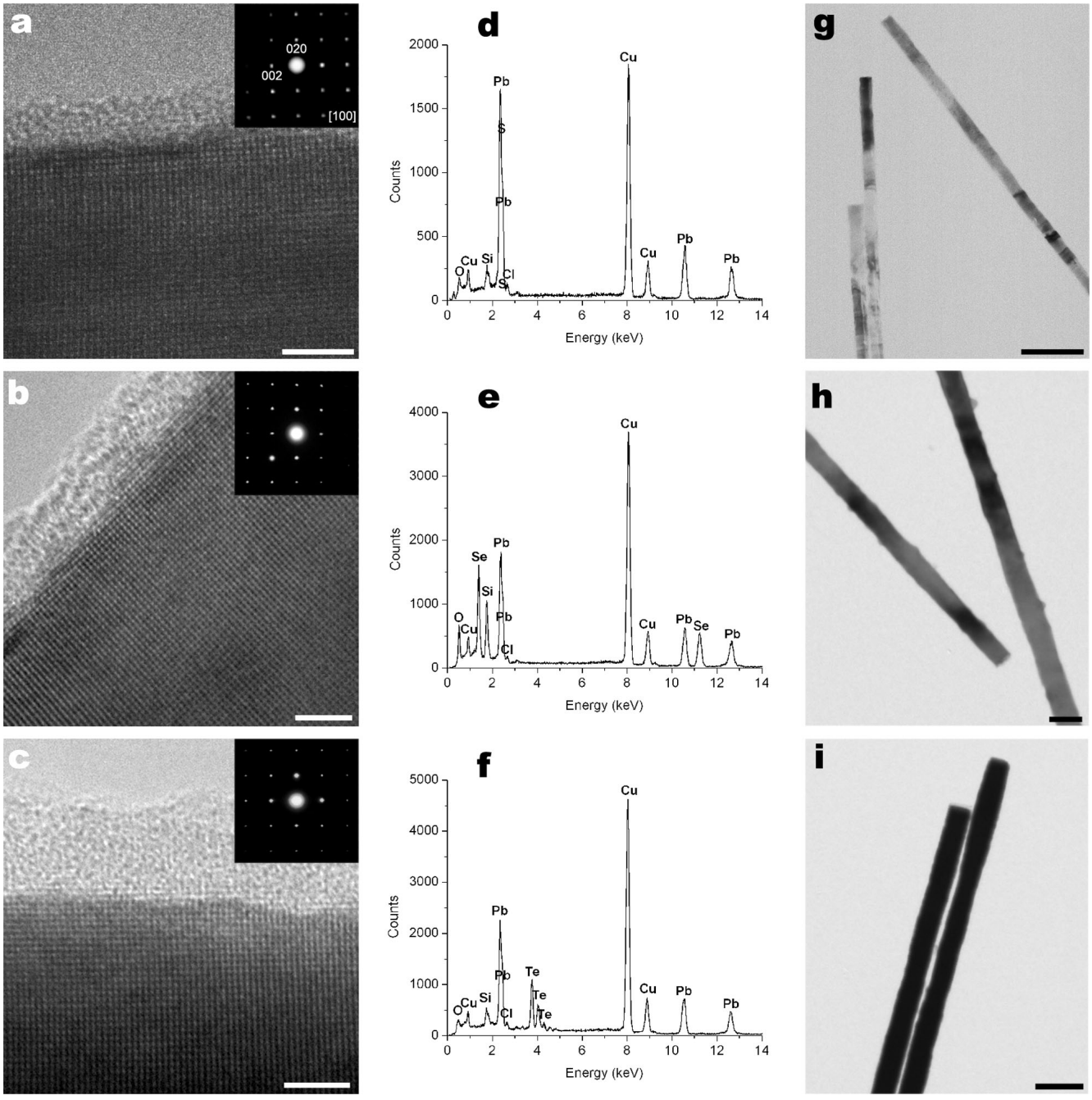

Figure 3. HRTEM images of a) PbS, b) PbSe, and c) PbTe nanowires showing their crystalline nature as well as the amorphous SiO_2 coatings. Scale bars are 3 nm. Insets are SAED patterns of each material taken from the [100] zone axis indicating that the nanowires grew in the <100> directions. EDX spectra from d) PbS, e) PbSe, and f) PbTe nanowires, confirming their purity. TEM images of g) PbS, h) PbSe, and i) PbTe nanowires displaying typical diameters. Scale bars are 500 nm, 100 nm, and 500 nm, respectively.

as determined from the transconductance plot of the data. *I–V* data was also taken from an 83 nm PbTe nanowire. A roughly linear *I–V* curve was obtained, which is indicative of nearly ohmic contacts. Unlike PbS devices, the PbTe device only weakly gates, due to its higher carrier concentration of 8.4×10^{19} cm^{-3}. This device is p-type and has a resistivity of 0.1 Ω cm and a mobility of 0.71 $cm^2 V^{-1} s^{-1}$. Several PbSe nanowire devices were measured, and with an average wire diameter of 95 nm, the wires have an average resistivity of 0.15 Ω cm, though some samples exhibit resistivities below 1×10^{-2} Ω cm. Mobility and carrier concentration values for the PbS and PbTe devices were determined using the standard back-gate nanowire transistor formulas derived from the cylinder-on-plate electrostatic model.[22] This model neglects the influence of contact resistance, surface trap states, and poor gating efficiency across the nanowire width,[23] thus causing

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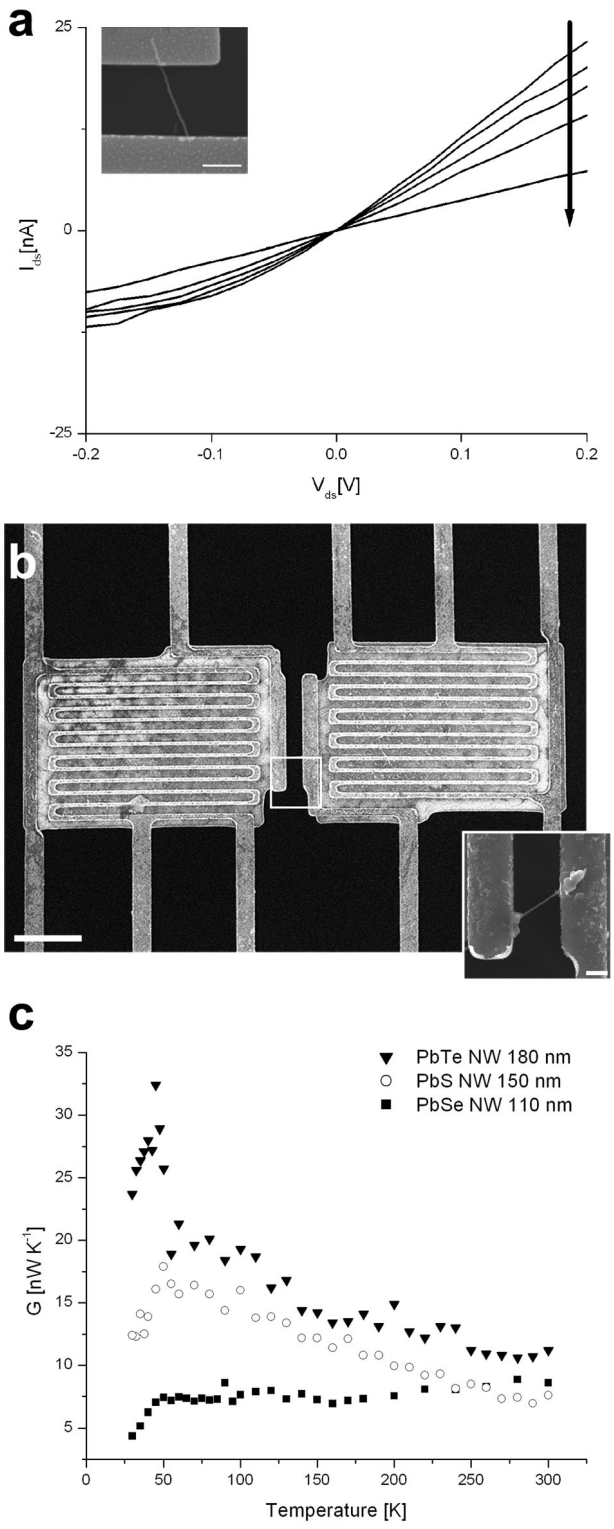

Figure 4. a) *I–V* characteristics of a 63 nm PbS nanowire. Gate voltages are 15, 10, 5, 0, and –5 V and increase in the direction of the arrow. Inset is an SEM image of the electrical device, scale bar is 1 μm. b) SEM image of a nanowire bridging two suspended heating pads for thermal conductance measurement, scale bar is 10 μm. Inset is the bridging nanowire highlighted in the main figure, scale bar is 500 nm. c) Temperature-dependent thermal conductance of a PbS, PbSe, and PbTe nanowire. The nanowire diameters are 150 nm, 110 nm, and 180 nm, respectively.

these values to be a lower estimate of the true semiconductor mobility. Moreover, it is conceivable that higher mobility values can be achieved by carrier concentration reduction as well as surface passivation.

In order to measure the thermal conductivity of these materials, individual nanowires were thermally bonded between suspended heating and sensing pads, as described previously.[3] The pads consist of suspended SiN_x membranes with Pt lines patterned on top (Fig. 4b). Each pad has a Pt coil and four contact lines to make four-point measurements of the coil resistance. One pad is heated by passing a current through the Pt coil, ramping the temperature ~2–5 K above the ambient temperature. The increase in resistance of the other pad is used to calculate the temperature rise at the cold end of the wire. The difference in temperature between the two pads can be used to calculate the thermal conductance of the nanowire.

The thermal conductance (G) measurements shown in Figure 4c are from silica-coated PbS, PbSe, and PbTe nanowires. The thermal conductivity can be calculated from the conductance using the diameter of the nanowire and the conduction length between the two suspended membranes.[3] The nanowire diameters were measured from SEM images of bridging devices. Though the bulk materials have a similar temperature-dependent thermal conductivity, the effects of phonon confinement can be seen as the nanowire diameter decreases. Even at 180 nm in diameter, the peak G of the PbTe nanowire is shifted out to 40 K as compared to 10 K in bulk.[24] The peak G of the 150 nm PbS nanowire occurs near 50 K, while the 110 nm PbSe nanowire has no apparent peak whatsoever. G of the PbSe nanowire is highest when it reaches 9 nW K^{-1} at 300 K.

Using dimensions measured from SEM images, the thermal conductivity of the PbSe nanowire is estimated to be lower than those of bulk PbSe at the same temperatures by a factor of 10–1000.[24] The conductivity plateaus above 50 K, and approaches the bulk value near room temperature.[19] The peak in bulk thermal conductivity occurs when normal and Umklapp phonon-phonon scattering processes dominate other scattering mechanisms, such as boundary and impurity scattering.[3] In the PbSe nanowire, however, this transition shifts to higher temperatures because phonon scattering at the nanowire surface or $PbSe/SiO_2$ interface dominates thermal transport over a much larger temperature range.

In the Si nanowire case,[3] thermal conductivity values even above 300 K are significantly lower than the bulk values due to strong boundary scattering. This is not the case for the PbSe nanowire, and in light of the fact that the phonon mean free path in bulk PbSe[5] is significantly shorter than in Si, phonon transport may be operating in an intermediate regime at the PbSe nanowire size scale. The significant increase in phonon scattering as compared to bulk at low temperatures—when phonon mean free paths are long—and the regression to bulk scattering processes as the mean free path drops below the nanowire diameter, suggest a smaller diameter nanowire may be necessary to effectively scatter phonons at high temperatures. Nonetheless, the large disparity between nano-

wire and bulk thermal transport below 100 K may improve the ZT of nanowire-based PbX materials in this temperature region.

In summary, lead chalcogenide nanowire arrays have been synthesized by a CVT method. XRD, SEM, HRTEM, SAED, and EDX were used to characterize the nanowire structures, and they were found to be single crystalline. This CVT method is equally applicable to PbS, PbSe, and PbTe nanowire synthesis, and may possibly be extended to PbX alloy nanowire systems for better engineering of phonon scattering. The thermal conductivity of PbSe nanowires is greatly diminished from the bulk PbSe values below 100 K, and may significantly increase the overall efficiency of these materials in this temperature region. In order to accurately gauge their potential as novel thermoelectric materials, future experiments should include Seebeck coefficient measurements. The decrease in thermal conductivity of two to three orders of magnitude suggests that nanowire systems of promising thermoelectric bulk materials could potentially push the upper limits of their ZT values.

Experimental

Materials: $PbCl_2$ (Alfa Aesar, 99 %), S powder (Alfa Aesar, –325 mesh, 99.5 %), amorphous Se powder (Alfa Aesar, –325 mesh, 99.999 %), and Te powder (Alfa Aesar, –200 mesh, 99.5 %) were used as received. Single-crystalline Silicon (100) wafers were cut into substrates approximately 1×3 cm^2. All substrates were cleaned with isopropanol and dried under a N_2 stream.

Synthesis of PbS: Experimental apparatus for all syntheses consisted of a quartz tube inside a Lindberg/Blue horizontal tube furnace. A typical synthesis for PbS nanowires follows: 0.80 g $PbCl_2$ and 0.33 g S were loaded into separate alumina boats. The $PbCl_2$ boat was positioned directly in the middle of the furnace where the temperature could be strictly controlled. The S boat was placed 3 cm from the center on the upstream side. Several Si (100) substrates were positioned on the downstream side 5–16 cm from the center. Prior to deposition, the tube was purged with carrier gas for 30 min at room temperature to remove oxygen from the reaction environment. The tube was heated between 600–700 °C for 10 min under 45–80 sccm of N_2, 5 % H_2 balance N_2, Ar, or 10 % H_2 balance Ar. After heating, the tube was allowed to cool to room temperature.

Synthesis of PbSe Nanowires: The PbS synthesis procedure was used except for the following adjustments: 0.57 g of $PbCl_2$ and 0.45 g of Se were loaded into the tube with the Se boat 3.5 cm from the center on the upstream side. The precursors and Si substrates were heated to 900–950 °C under 5–60 sccm of carrier gas flow.

Synthesis of PbTe Nanowires: The PbS synthesis procedure was used except for the following adjustments: 0.57 g $PbCl_2$ and 0.57 g Te were inserted into the tube with the Te boat 4 cm upstream from the center. The tube was heated to 800–900 °C under 5–125 sccm of carrier gas flow.

Characterization: XRD patterns were taken on a Co Kα Bruker D-8 GADDS diffractometer. The SEM and TEM analyses were performed using a JEOL JSM-6340F Field Emission SEM and a Philips CM 200 FEG, respectively. Samples for TEM characterization were prepared by contact transfer onto 200 mesh carbon-coated copper grids.

Electrical Measurement: For electrical devices, nanowires were sonicated into isopropanol, and the suspension was drop-cast onto substrates. The substrates consisted of prefabricated Au probe-pad electrodes on top of a degenerately p-doped Si wafer with 350 nm Si_3N_4 gate dielectric that was deposited using a low-pressure chemical vapor deposition Tystar furnace. The substrates were then soaked in 10:1 BHF to selectively remove the insulating silica coating on the outer surface of the nanowires. After spinning a PMMA layer onto the substrates, EBL contacts were generated using a JEOL series 6400 SEM and Nanometer Pattern Generation System (NPGS). The exposed PMMA regions were developed with a methyl isobutyl ketone:isopropanol (1:3) mixture and the substrates were washed for 5 seconds in 10:1 BHF and rinsed for 12 seconds in deionized water. The devices were cleaned using oxygen plasma for 60 s at 50 W. 5 nm Pd, 3 nm Ti, 200 nm Pd, and 50 nm Au were deposited sequentially onto the exposed substrate by electron-beam evaporation.

Thermal Measurement: To prepare thermal devices, substrates containing nanowires were briefly sonicated in isopropanol, and the suspension was drop-cast onto chips containing arrays of microfabricated thermal measurement devices. Individual nanowires bridging the heating and sensing pads were thermally anchored to the suspended membranes by electron beam-induced decomposition of a Pt precursor using an FEI Strata 235 Dual Beam FIB. The external contact pads were wire-bonded to a 24-pin chip package and placed in a liquid Helium-cooled Lake Shore ST100 cryostat for measurement.

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[1] A. Majumdar, *Science* **2004**, *303*, 777.
[2] L. D. Hicks, M. S. Dresselhaus, *Phys. Rev. B* **1993**, *47*, 12 727.
[3] D. Li, Y. Wu, P. Kim, L. Shi, P. Yang, A. Majumdar, *Appl. Phys. Lett.* **2003**, *83*, 2934.
[4] M. S. Dresselhaus, G. Dresselhaus, X. Sun, Z. Zhang, S. B. Cronin, T. Koga, J. Y. Ying, G. Chen, *Microscale Thermophys. Eng.* **1999**, *3*, 89.
[5] Y.-M. Lin, M. S. Dresselhaus, *Phys. Rev. B* **2003**, *68*, 075 304.
[6] D. A. Broido, T. L. Reinecke, *Appl. Phys. Lett.* **1997**, *70*, 2834.
[7] R. Venkatasubramanian, E. Siivola, T. Colpitts, B. O'Quinn, *Nature* **2001**, *413*, 597.
[8] H. Beyer, J. Nurnus, H. Böttner, A. Lambrecht, T. Roch, G. Bauer, *Appl. Phys. Lett.* **2002**, *80*, 1216.
[9] J. P. Heremans, C. M. Thrush, D. T. Morelli, *Phys. Rev. B* **2004**, *70*, 115 334.
[10] T. C. Harman, P. J. Taylor, M. P. Walsh, B. E. LaForge, *Science* **2002**, *297*, 2229.
[11] F. Gao, Q. Lu, X. Liu, Y. Yan, D. Zhao, *Nano Lett.* **2001**, *1*, 743.
[12] K.-S. Cho, D. V. Talapin, W. Gaschler, C. B. Murray, *J. Am. Chem. Soc.* **2005**, *127*, 7140.
[13] K. L. Hull, J. W. Grebinski, T. H. Kosel, M. Kuno, *Chem. Mater.* **2005**, *17*, 4416.
[14] E. Lifshitz, M. Bashouti, V. Kloper, A. Kigel, M. S. Eisen, S. Berger, *Nano Lett.* **2003**, *3*, 857.
[15] C. Zhang, Z. Kang, E. Shen, E. Wang, L. Gao, F. Luo, C. Tian, C. Wang, Y. Lan, J. Li, X. Cao, *J. Phys. Chem. B* **2006**, *110*, 184.
[16] L. Zhang, J. C. Yu, M. Mo, L. Wu, K. W. Kwong, Q. Li, *Small* **2005**, *1*, 349.
[17] Y. Liu, J. Cao, J. Zeng, C. Li, Y. Qian, S. Zhang, *Eur. J. Inorg. Chem.* **2003**, 644.
[18] J.-P. Ge, J. Wang, H.-X. Zhang, X. Wang, Q. Peng, Y.-D. Li, *Chem. Eur. J.* **2005**, *11*, 1889.
[19] Y. I. Ravich, B. A. Efimova, I. A. Smirnov, *Semiconducting Lead Chalcogenides*, Monographs in Semiconductor Physics, Vol. 5 (Ed: L. S. Stil'bans), Plenum, New York **1970**.
[20] M. Afzaal, P. O'Brien, *J. Mater. Chem.* **2006**, *16*, 1113.
[21] H.-X. Zhang, J.-P. Ge, Y.-D. Li, *Chem. Vap. Deposition* **2005**, *11*, 147.
[22] J. Goldberger, D. J. Sirbuly, M. Law, P. Yang, *J. Phys. Chem. B* **2005**, *109*, 9.
[23] D. Vashaee, A. Shakouri, J. Goldberger, T. Kuykendall, P. Pauzauskie, P. Yang, *J. Appl. Phys.* **2006**, *99*, 054 310.
[24] D. Greig, *Phys. Rev.* **1960**, *120*, 358.