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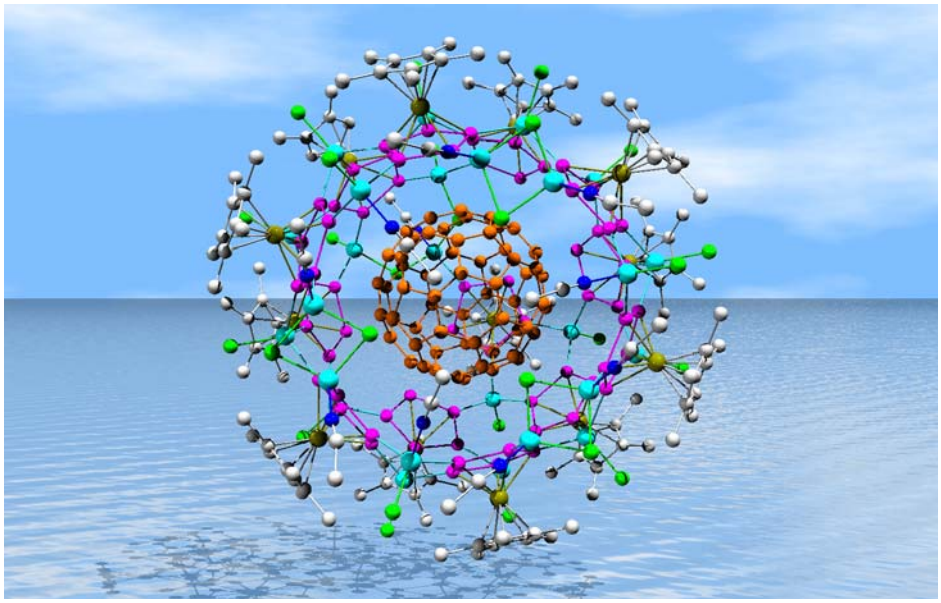

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Papers published in this issue include:

Chemistry and physics of silicon nanowire†

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This article provides a short overview of the current status of the silicon nanowire research including its synthetic chemistry and physical property characterization, with examples drawn mainly from the author's lab.

Introduction

Group IV semiconductors have been central to many technological innovations for decades, and remain to be unsubstitutable key materials for electronic industry. They pose to be the primary candidate for the next generation of nanoelectronics. Micro- and nanofabrication techniques have enabled a highly reliable production of well-defined and sophisticated structures down to sub-100 nm scale. The conventional top-down fabrication, however, is running into fundamental limitations in fabrication of molecular scale nanostructures. Alternatively, bottom-up synthetic chemistry is able to produce complex nanostructures *via* self-assembly of nanocrystals, nanowires or nanotubes.[1,2] Silicon nanotructures have garnered the greatest attention in the past decade for a variety of applications including nanoelectronics and energy conversion. Horizontal and vertical silicon nanowire field effect transistors (FETs),[3,4] complementary logic gates,[5] nanoelectromechanical systems (NEMS),[6,7] bio-chemical sensors[8,9] and various energy conversion devices[10–12] have been reported. In this article, I would like to provide a short survey of recent research efforts on Si nanowires, mainly focusing on results obtained in my own research group.

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The vapor–liquid–solid process for Si nanowires

Si or Ge nanowires are typically synthesized by chemical vapor deposition (CVD) *via* the vapor–liquid–solid (VLS) process.[13] The basic principle underlying the VLS process is the precipitation of one material from a supersaturated liquid alloy. With silicon nanowire growth as example, it typically involves several growth steps: (1) diffusion of Si species from the vapor source to the vapor/Au–Si liquid interface; (2) diffusion and/or surface reaction on the vapor/liquid interface; (3) diffusion in the liquid droplet; (4) precipitation of Si at the liquid/nanowire interface. This VLS nanowire growth was first observed by Wu and coworkers in real time in a high temperature transmission electron microscope.[14]

$SiCl_4$ and SiH_4 are two commonly used precursors to produce Si thin films in semiconductor technology and are naturally adopted for the synthesis of Si nanowires. A typical reaction system is schematically shown in Fig. 1. With a good understanding of the VLS growth mechanism, it is now possible to grow high quality Si, Ge, alloy SiGe as well as their superlattice nanowires[15] by rational design of precursor delivery process in the vapor deposition system.

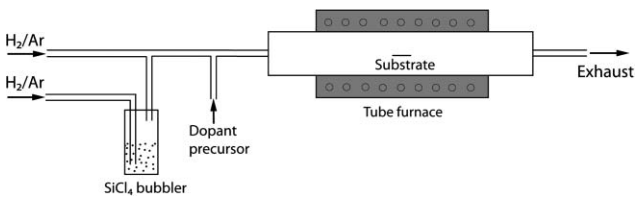

Fig. 1 Schematic drawing of the VLS experimental set-up.

It is desirable to have the capability to control the diameters of nanowires for diameter dependent studies and device applications. Based on the VLS mechanism, this can be readily achieved by controlling the size of the alloy droplets, and essentially, the size of the metal particles. A very common method is to use monodispersed metal nanoparticles (*e.g.* Au, Pt) for nanowire growth.[16,17] This strategy can now readily produce silicon nanowires with controllable diameters down to sub-10 nm dimensions. Silicon nanowires typically grow along the <111> direction, but when the diameter of nanowires is smaller than 20 nm, many of them would take the <110> growth direction (Fig. 2).

Due to their preferred growth direction, epitaxial alignment and orientation selection are the characteristics for the epitaxial growth of Si nanowires on Si substrates. Particularly for nanowires

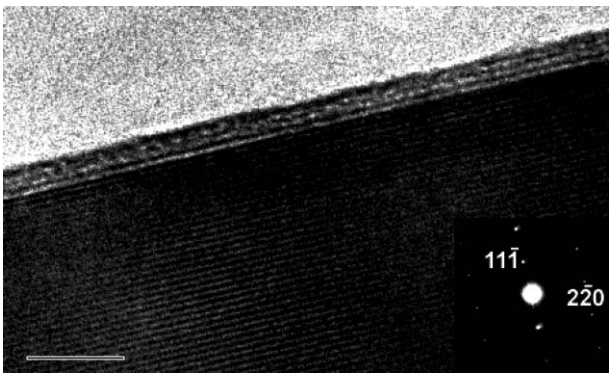

Fig. 2 High resolution TEM image for a <110> oriented Si nanowire. The image and the diffraction pattern are taken along the [112] zone axis, so the (11$\bar{1}$) plane is parallel to the electron beam and its flatness is shown at the edge. Scale bar, 4 nm.

with the <111> growth direction grown on (111) substrates, the orientation typically favors the perpendicular one, providing a reliable means for orientation control. We have also explored a silicon-on-insulator (SOI) strategy to grow Si nanowire bridge structures.[18] If the (111) surface is oriented vertically, <111> nanowires would grow laterally. If there is an opposite vertical (111) surface facing the growing nanowires, the nanowires will eventually reach and make a connection there, forming a nanowire bridge (Fig. 3). These vertical {111} surfaces can be obtained on Si (110) substrates using a one-step photolithography followed by vertical etching and will give trench structures with {111} sidewalls. Following the standard growth procedure for planar substrates using metal nanoparticles as the catalysts, we are able to get nanowires grown in the trenches on these specially prepared substrates. As shown in Fig. 3, the nanowires in trench grow laterally and perpendicularly to the exposed {111} vertical surface. It is worth noting that the orientation has rather large tolerance of the misalignment of trench walls and the surface roughness caused by etching. For example, although scalloping formed in etching exists on the surfaces (~500 nm in period), nanowires persist to grow perpendicularly to these side surfaces.[7]

Integration of silicon nanowire into vertical field effect transistors

Silicon nanowires have received considerable attention as future transistor components because they represent a facile route towards sub-100 nm single-crystalline Si features with minimal surface roughness. Typically, silicon nanowire transistors have a horizontal planar layout with either a top or back gate geometry. Pushing the transistor geometry into the third dimension would result in ultra-high transistor densities. In addition, a vertical nanowire geometry also promises enhanced transistor performance due to the enhanced gate control efficiency in its surround-gate design. We have successfully demonstrated the integration of vertically grown Si nanowire arrays into vertical field effect transistors with a surround-gate architecture. These first-generation vertically-integrated nanowire field-effect-transistors (VINFETs) exhibit electronic properties that are comparable to other horizontal nanowire FETs and traditional metal-oxide silicon field effect transistors (MOSFETs), suggesting that further

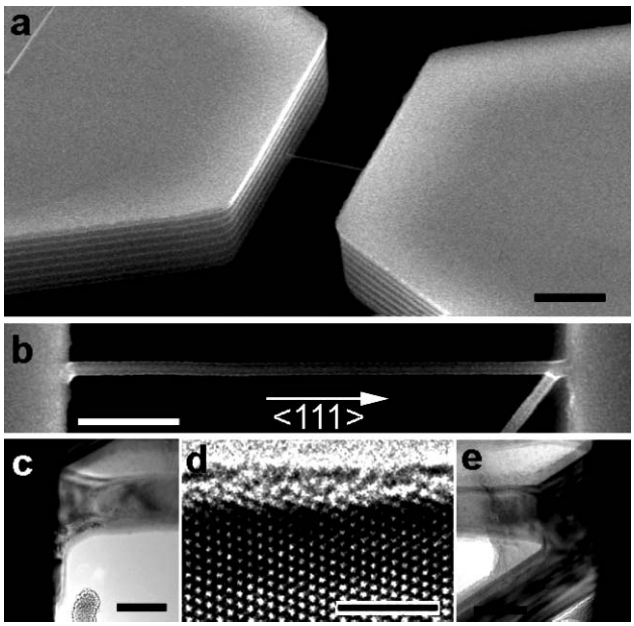

Fig. 3 <111> oriented Si nanowire bridges on silicon-on-insulator substrates. (a) A single nanowire with <111> growth direction is bridging in a trench confined by vertical {111} faces on a <110> oriented SOI substrate. The parallel lines on the sidewalls with alternating contrast are scallops formed in deep reactive ion etching. (b) The general morphology of a bridged nanowire. It grew from the left sidewall along the <111> direction and impinged into the opposite sidewall; it finally grew backwards after self-welding into the sidewall. (c) and (e) Cross section TEM images for the two joints between a nanowire and trench sidewalls. (d) HREM image confirms the <111> growth direction and reveals a thin oxide layer on the surface of the nanowire. Scale bars: (a) 2 μm; (b) 500 nm; (c) and (e) 100 nm; (d) 3 nm. [Adapted from ref. 7.]

optimization of this device structure may make them competitive with advanced solid state electronic devices for future nanoelectronic devices.

Fig. 4a shows a cross-sectional view of our nanowire VINFET device.[4] These devices are fabricated using conventional very-large-scale integration (VLSI) processing, but without the need for post-growth nanowire assembly. The vertically grown silicon nanowires were thermally oxidized to create uniform thermal

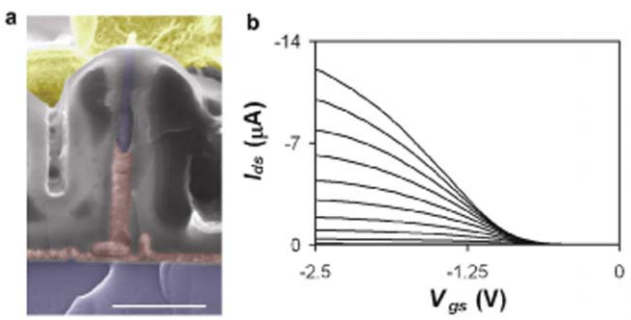

Fig. 4 VINFET device configuration and characteristics. (a) Cross-sectional SEM image of a VINFET device. Scale bar is 500 nm. False color is added to the image for clarity. Blue corresponds to the Si source and nanowire, grey corresponds to SiO_2 dielectric, red corresponds to the gate material, and yellow corresponds to the drain metal. (b) VINFET device I_{ds} *vs* V_{gs} with V_{ds} ranging from −2.5 to −0.25 V in 0.25-V steps, from top to bottom, respectively. [Adapted from ref. 4.]

oxides as dielectrics. A typical device has a ~20–30 nm Si nanowire diameter, surrounded by ~30–40 nm of high-temperature gate oxide, and a Cr metal gate length of ~500–600 nm, and nanowire channel lengths that range from ~1.0 to 1.5 μm. The significant figures of merit for transistor performance include the transconductance (g_m), the device mobility (μ), on–off current ratio (I_{on}/I_{off}), and the subthreshold slope (S). The g_m for our VINFET devices ranged from 0.2 to 8.2 μS. The hole mobilities range from 7.5 to 102 $cm^2\ V^{-1}\ s^{-1}$ with an average mobility of 52 $cm^2\ V^{-1}s^{-1}$. I_{on}/I_{off} ranges from 10^4 to 10^6 for all devices (Fig. 4b). Finally, the minimization of the subthreshold slope is necessary for low power switching applications in digital electronics. The S value for a typical device having a 300 Å gate oxide shell is 120 mV $decade^{-1}$.

Our prototype Si VINFET devices represent a novel platform for silicon nanowire electronics that combines the epitaxial growth of silicon nanowires with top–down fabrication. Future optimization of the processing, device geometry, doping concentration, the use of high-k dielectrics, as well as reduction of the gate length may make these devices competitive with FINFETs and other current advanced solid state devices in the sub-10 nm regime. The transistor density per unit area could be further increased through fabricating multiple gate electrodes and source/drain connections along the length of an individual nanowire (*i.e.* stacking devices on single nanowires), taking advantage of our high aspect ratio vertical nanowire conduction channel. Also, the ability to incorporate longitudinal and co-axial heterostructures into these nanowires should allow additional future design flexibility, such as the on-chip incorporation of vertical SiGe heterostructures, for on-chip thermoelectric cooling.

The performance of these silicon nanowire field effect transistors can be further improved through proper surface functionalization. For example, we have demonstrated that Si nanowires modified by covalent Si–CH_3 functionality,[19] with no intervening oxide, show excellent atmospheric stability, high transconductance values, low surface defect levels, and allow for the formation of air-stable Si nanowire FET's having on–off ratios in excess of 10^5 over a relatively small gate voltage swing (±2 V).

Giant piezoresistance effect in silicon nanowires and nanowire resonators

Application of a strain to a crystal results in a change in electrical conductivity due to the piezoresistance effect (change of resistivity with stress/strain). The piezoresistance effect of silicon has been widely utilized in mechanical sensors for half a century and is now being actively explored in order to improve the performance of silicon transistors. We have recently discovered that Si nanowires possess unusually large piezoresistance effect compared to bulk.[7] For example, the longitudinal piezoresistance coefficient along the <111> direction increases with decreasing diameter for p-type Si nanowires, reaching as high as $-3550 \times 10^{-11}\ Pa^{-1}$ while the value for bulk is $-94 \times 10^{-11}\ Pa^{-1}$. In order to evaluate the piezoresistance effect (or electromechanical properties) in nanostructures, mechanical manipulations and electrical measurements must be performed simultaneously. The nanowire-in-microtrench architecture on a SOI wafer (Fig. 3) is ideally suited for this purpose. We found that the significant enhancement of the piezoresistance effect is not limited to the <111> direction. The measurements on <110> oriented Si nanowires also show very large longitudinal coefficient. For example, it was measured to be $-660 \times 10^{-11}\ Pa^{-1}$ for a 75 nm thick nanowire with resistivity of 0.3 Ω cm (the bulk value for p-type Si is $-70 \times 10^{-11}\ Pa^{-1}$ for the same resistivity). Systematically theoretical calculations are required to reveal the underlying mechanisms for the observations. This enhanced piezoresistance effect could find applications in Si nanotechnology, flexible electronics as well as in nanoelectromechanical systems (NEMS).

Typical NEMS resonators are made by a top–down lithographic techniques and surface nanomachining, which together enable realization of nanomechanical devices with considerable complexity and functionality. These high frequency nanomechanical resonators are being actively explored for applications including resonant sensors for ultra-high resolution mass sensing, force detection, quantum electromechanics, electromechanical signal generation and processing, and high-speed logic and computation. On the other hand, our chemical-synthesis-based bottom-up approaches now provide nanowires with high crystalline quality, perfectly terminated surfaces, and sizes down to the molecular scale. These represent a new class of building blocks for NEMS resonators that offer unique attributes. Our nanowire-in-microtrench device geometry facilitates the direct probing of mechanical properties of Si nanowires *via* static deflection. We have developed resonant mechanical devices operating at very high frequencies (VHF) that are based on our suspended Si nanowires.[6] Metallized Si nanowire resonators operating near 200 MHz can be realized with quality factor $Q \approx 2000$~2500. Pristine Si nanowire resonators, with fundamental resonances as high as 215 MHz, have also been measured. The pristine resonators provide the highest Q's, as high as $Q \approx 13100$ for an 80 MHz device. These high frequency nanowire resonators could serve as excellent platform for mass sensing; characterization of their mass responsivity and frequency stability demonstrates sensitivities approaching 10 zg.

Silicon nanowire based thermoelectrics

Phonon transport is expected to be greatly impeded in thin (*i.e.*, $d < \Lambda$, where d is the diameter and Λ is the phonon mean free path) nanowires as a result of increased boundary scattering and reduced phonon group velocities stemming from phonon confinement. Size-dependent thermal conductivity in nanostructures presents a major hurdle in the drive toward miniaturization in the semiconductor industry. Yet poor heat transport is advantageous for thermoelectric materials, which are characterized by a figure of merit ($ZT = \alpha^2 T/[\rho(\kappa_p + \kappa_e)]$, with α, T, ρ, κ_p and κ_e the Seebeck coefficient, absolute temperature, electronic resistivity, lattice thermal conductivity and electronic thermal conductivity, respectively) that improves as phonon transport worsens. A decade ago, the Dresselhaus group[20] predicted that ZT can be increased above bulk values in thin nanowires by carefully tailoring their diameters, compositions and carrier concentrations. This prediction has now been experimentally confirmed in my research group as well as in another Caltech research group.[11,12]

Thermal conductivity through individual nanowires can be measured with a suspended heater microdevice, which consists of two silicon nitride (SiN_x) membranes.[21,22] A Pt thin coil, acting as both resistive heater and thermometer, and a separate Pt electrode were patterned on each membrane and electrically connected to

contact pads by metal lines on the suspended legs. Nanowires were dispersed from solution to bridge two suspended membranes and amorphous carbon films were locally deposited at the nanowire-heater pad junctions with a scanning electron microscope. Shown in Fig. 5 are the measured thermal conductivities for intrinsic single-crystalline Si nanowires of different diameters (22, 37, 56, and 115 nm). The measured thermal conductivities are about two orders of magnitude lower than that of the bulk and, as the wire diameter is decreased, the corresponding thermal conductivity is reduced. This clearly indicates that enhanced boundary scattering has a strong effect on phonon transport in Si nanowires.

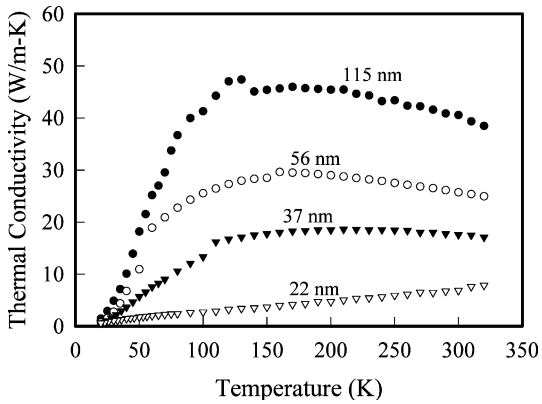

Fig. 5 Thermal conductance of Si nanowires. Measured thermal conductivity of different diameter Si nanowires. The number beside each curve denotes the corresponding wire diameter. [Adapted from ref. 21.]

More recently, we have developed a wafer-scale electrochemical synthesis of large-area arrays of rough Si nanowires that are 20–300 nm in diameter. These nanowires have S and ρ that are the same as in bulk doped Si, but those with diameters ~50 nm exhibit 100-fold reduction in k (= 1.6 W m^{-1} K^{-1}), which yields a large $ZT = 0.6$ (Fig. 6) at room temperature. Although bulk Si is a poor thermoelectric material, by greatly reducing k without significantly affecting S and ρ, Si nanowire arrays show promise as high-performance, scalable thermoelectric materials. With optimized doping, diameter reduction, and roughness control, the ZT is likely to rise even higher. This ZT enhancement can be attributed to efficient scattering throughout the phonon spectrum by the

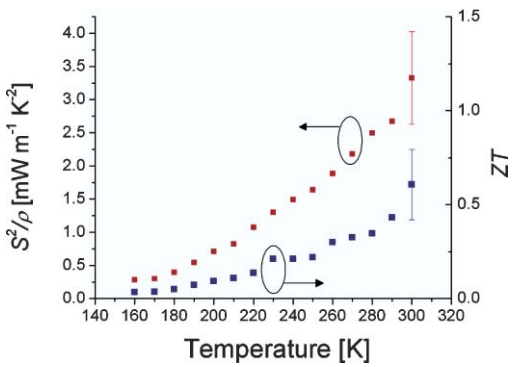

Fig. 6 Thermoelectric properties and ZT calculation for a rough silicon nanowire. Single nanowire power factor (red squares) of the nanowire and calculated ZT (blue squares) using the measured thermoconductivity of a 52 nm nanowire. [Adapted from ref. 11.]

introduction of nanostructures at different length scales (diameter, roughness, and point defects). The significant reduction in thermal conductivity may be a result of changes in the fundamental physics of heat transport in these quasi-one-dimensional materials. By achieving broadband impedance of phonon transport, we have demonstrated that the roughened Si nanowire system is capable of approaching the limits of minimum lattice thermal conductivity in Si. Thermoelectric energy conversion modules manufactured from such a ubiquitous material as Si, may find wide-ranging applications in waste heat salvaging, power generation, and solid-state refrigeration.

Future perspective

Silicon nanowire represents one of the most important research subjects in the nanowire research community. In the past ten years, many interesting physical properties have been discovered including, for example, giant piezoresistance effect, significantly reduced thermoconductivity and enhanced thermoelectric performance. These fundamentally new properties could eventually lead to significant breakthrough in their commercial applications. There are however still many important issues remaining to be addressed in the following years. These include, for example, low-cost large-scale production and assembly of high quality nanowires, precise doping and heterostructure formation in nanowire, reproducible surface and defect engineering of the nanowires, nano-macro interface and addressability issue. When our synthetic control on these nanostructures improves, novel and unexpected chemical and physical properties will arise. These novel nanostructures could have significant impact in electronics, photonics, energy conversion as well as other unexplored territories.

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