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Dopant profiling and surface analysis of silicon nanowires using capacitance–voltage measurements

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Silicon nanowires are expected to have applications in transistors, sensors, resonators, solar cells and thermoelectric systems[1–5]. Understanding the surface properties and dopant distribution will be critical for the fabrication of high-performance devices based on nanowires[6]. At present, determination of the dopant concentration depends on a combination of experimental measurements of the mobility and threshold voltage[7,8] in a nanowire field-effect transistor, a calculated value for the capacitance, and two assumptions—that the dopant distribution is uniform and that the surface (interface) charge density is known. These assumptions can be tested in planar devices with the capacitance–voltage technique[9]. This technique has also been used to determine the mobility of nanowires[10–13], but it has not been used to measure surface properties and dopant distributions, despite their influence on the electronic properties of nanowires[14,15]. Here, we measure the surface (interface) state density and the radial dopant profile of individual silicon nanowire field-effect transistors with the capacitance–voltage technique.

Figure 1a shows a schematic of a completed silicon nanowire field-effect transistor (FET) consisting of a single crystalline boron-doped silicon nanowire epitaxially bridging between highly doped silicon pads and electrically isolated from a silicon back-gate by a buried oxide layer. There is also an Al_2O_3 gate dielectric film covering the entire structure and a chromium metal gate line located in the trench between the silicon electrode pads and surrounding the nanowire. The device structure was fabricated by growing silicon nanowire bridges epitaxially across patterned silicon-on-insulator (SOI) trench substrates using gold nanoparticles and the vapour–liquid–solid (VLS) mechanism according to the methods in previous reports[16,17]. This patterning scheme, combined with the highly doped device layer, allows for integrated silicon contacts and facile silicon nanowire electrical measurements. The nanowire doping level was controlled by post-growth BCl_3 gas diffusion, and the Al_2O_3 gate dielectric was deposited by means of atomic layer deposition (ALD). The surround gate metal was patterned using photolithography and chromium sputtering.

Figure 1b shows a scanning electron micrograph (SEM) of a completed device that is close to the idealized device structure depicted in Fig. 1a; the inset is a tilted view of the device cross-section taken after focused ion beam (FIB) milling. The wire appears fully embedded in the surround gate metal and epitaxially integrated into the silicon electrodes. The cross-sectional SEM shows a distinct contrast difference between the bright chromium surround gate and the dark Al_2O_3 gate oxide, with a smaller contrast difference at the Si/Al_2O_3 interface. The silicon nanowire also shows hexagonal faceting, as expected for <111> oriented wires according to surface energy considerations, but the surfaces appear to be {211} instead of the theoretically predicted {110} facets[18]. Most studies aimed at calculating silicon nanowire cross-sectional shapes only consider the low index {110}, {111} and {100} as possible facets to reduce the number of permutations, but {211} bounded nanowires should also be possible and have been commonly observed in micrometre-scale <111> oriented whiskers grown using the VLS mechanism[19]. The dimensions extracted from the cross-sectional and plan-view SEM lead to a chromium gate length of 2.3 μm, a silicon nanowire diameter of ~75 nm, and Al_2O_3 thickness of ~15 nm, consistent with transmission electron microscopy (TEM) observations of other wires on the sample. The surround gate horizontal silicon nanowire FET structure achieved here represents the ideal geometry for optimal electrostatic control of the wire section located underneath the metal line, while also allowing for independent tuning of the carrier concentration by means of the back-gate in the two nanowire leads not embedded in metal. The capacitance–voltage (C–V) instrument setup is similar to the configuration used recently for carbon nanotube quantum capacitance measurements[20].

Figure 2a shows the silicon nanowire C–V response at 200 Hz, 2 kHz and 20 kHz with the back-gate set at –20 V to make the leads very conductive and the background C–V taken with the back-gate at 8 V set as the baseline. All of the measurements were taken at 77 K. The C–V curves show saturation to an oxide capacitance of 2.5 fF at negative gate bias and 0.5 fF at positive bias. There is significant frequency dispersion in the depletion region, leading to a substantial shift between the high- and low-frequency curves. The increased low-frequency capacitance in the depletion region is typically attributed to interface states that cannot respond quickly enough to the high-frequency a.c. voltage signal and thus freeze out at increased frequency[9]. These states have some dispersion within the semiconductor bandgap, so as the gate voltage causes the Fermi level to scan from the valence band edge to the centre of the bandgap (accumulation through depletion to onset of inversion) they can be populated or depopulated, depending on whether they are acceptor- or donor-type states. Therefore, we can extract the interface state density D_{it} as a function of position in the bandgap by comparing the high- and low-frequency capacitance curves at various gate bias values (see Supplementary Information)[9].

Figure 2b shows the resulting D_{it} versus bandgap energy plot, which varies from 4×10^{11} cm^{-2} eV^{-1} at mid-gap to 1×10^{13} cm^{-2} eV^{-1} closer to the band edge. This matches well with results on planar silicon; the mid-gap density is about an order of magnitude above high-quality thermal oxide interfaces, but similar to both literature and planar control experiment values for Al_2O_3 on silicon (see Supplementary Information)[21–23]. The shape

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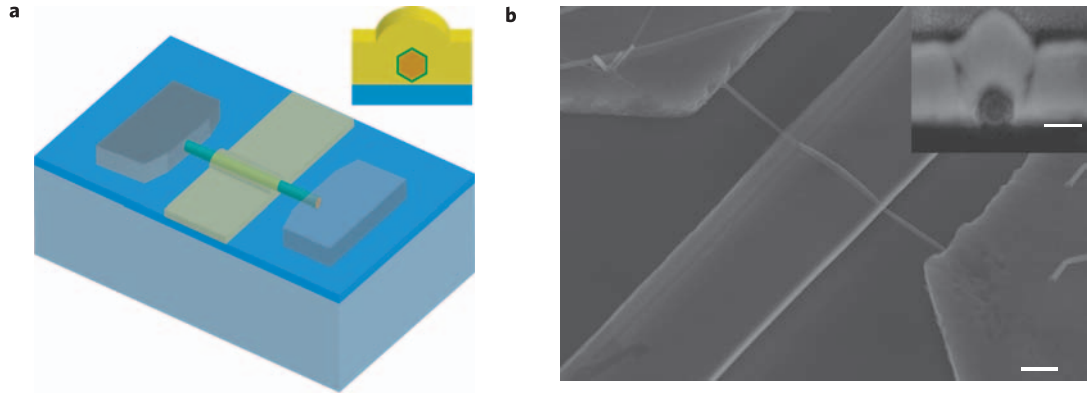

Figure 1 | Device structure. a, Schematic of the C–V device structure with p^+-Si source and drain pads (grey), SiO_2 buried oxide (blue), p^+-Si back-gate (grey), p-Si NW (orange), ALD Al_2O_3 surround gate oxide (green) and chromium surround gate metal (yellow). Inset: cross-sectional schematic view with a hexagonally faceted silicon nanowire. **b**, SEM image of an actual nanowire device. Inset: a cross-sectional view of the device taken after focused ion beam (FIB) milling. Scale bars; 1 μm and 100 nm.

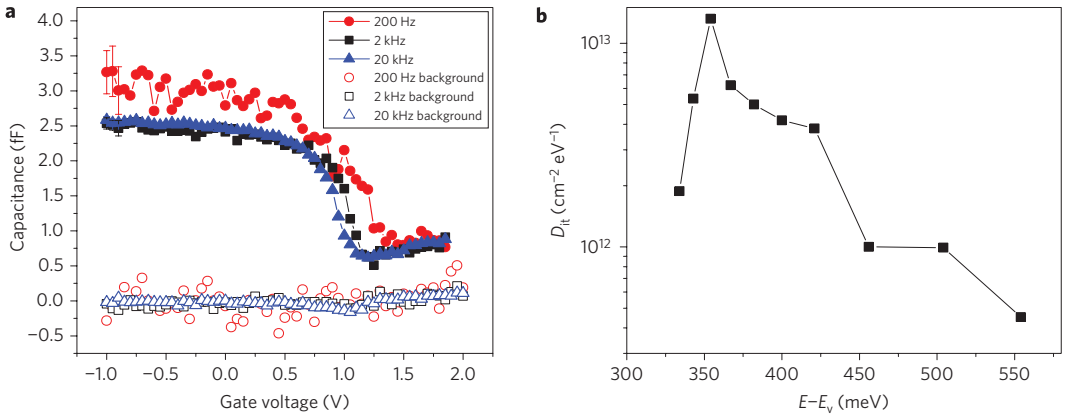

Figure 2 | Capacitance–voltage frequency-dependent measurements. a, Capacitance–voltage curves measured at 77 K and 200 Hz (red circles), 2 kHz (black squares) and 20 kHz (blue triangles), with the background shown by the corresponding open symbols. The error bars are shown only for the first three data points for clarity. **b**, Interface state density D_{it} versus position in the bandgap with respect to the valence band extracted from the 200 Hz and 20 kHz C–V curves using the high–low method.

of the D_{it} curve and peak position within several hundred meV of the valence band edge are also qualitatively similar to what has been observed in planar silicon junctions[9,22]. The comparable D_{it} values despite the large number of edge sites in nanowires compared to planar surfaces probably indicate ideal surface faceting and very low surface roughness, as observed previously for VLS-grown silicon nanowires[17,24,25]. It is also possible that there are some very slow or very fast interface states that we cannot probe in our 200 Hz to 20 kHz frequency range. The high–low method is well known to underestimate the interface state density due to the difficulties in obtaining true high- and low-frequency behaviour, so the measured values represent a lower bound to the true D_{it} value; however, from previous studies on planar silicon we expect no more than a factor of two difference from the true profile[9,26]. This technique is very powerful, as it allows us to decouple interface state effects from other influences that have been shown to have a dramatic effect in nanowire transport properties such as strain, chemical gating through surface charges, and surface roughness[1,5,17].

We have also extracted the dopant profile using the high-frequency C–V curve. The principle behind dopant profiling is that as the nanowire becomes depleted, the effective insulator thickness increases and the capacitance drops. The voltage dependence of this drop is related to the majority carrier (and thus dopant) density; a rapid drop indicates a low dopant concentration, whereas a slow reduction indicates a high doping level (see Supplementary Information for details). Figure 3a shows the expected dopant diffusion profile simulated using the experimental doping conditions as inputs (N_a—diffusion). Starting with this dopant profile, we used finite-element modelling (FEM) electrostatic simulations (Comsol Multiphysics) to calculate the corresponding majority carrier distribution (Fig. 3a; p(r)—diffusion) and the ideal C–V curve, assuming a surround gate FET with the dimensions taken from the experiment. We then extracted the majority carrier profile from both the ideal and experimental C–V curves (Fig. 3a; p(r)—simulation and p(r)—experimental, respectively; the extraction method is detailed in the Supplementary Information). All the majority carrier profiles show excellent agreement for most of the nanowire, with a density close to the boron solid solubility of 1×10^{19} cm^{-3} near the surface and dropping to $\sim 1 \times 10^{17}$ cm^{-3} near the wire core. They also match very well with the simulated dopant profile in the outer half of the nanowire, but start to diverge towards the core. This is expected according to the C–V dopant profile resolution limitation of twice the Debye screening length (L_d), which depends on dopant density, temperature and dielectric constant. At our measurement temperature of 77 K, L_d is ~2 and 13 nm at the nanowire surface and core, respectively[9]. Additionally, because the Fermi level depends on dopant concentration, some majority carriers will redistribute within the nanowire from the high to low dopant density regions. As C–V actually measures the free carriers and not the dopant

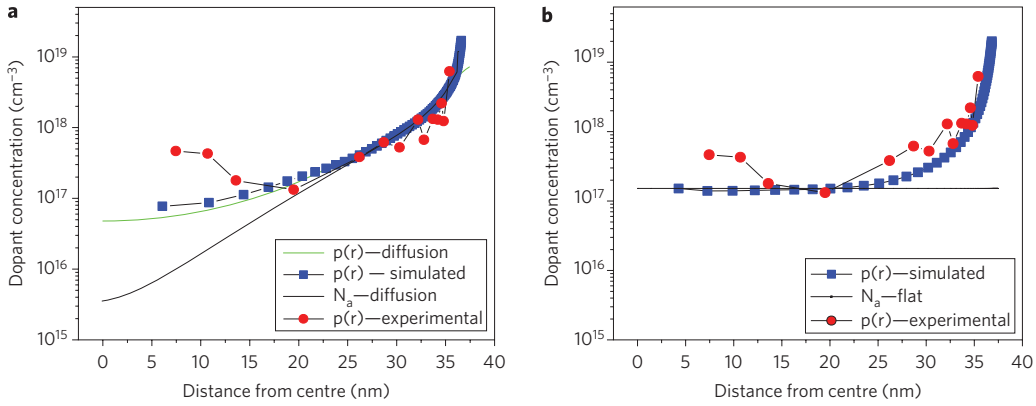

Figure 3 | Radial dopant profile. a, Radial dopant distribution extracted from the experimental C–V curve (red) compared to the simulated boron diffusion profile (black), the calculated majority carrier redistribution using the simulated dopant profile as an input (green), and the carrier concentration extracted from the theoretical C–V curve with the simulated boron profile as an input (blue). **b**, The same curves compared for a flat boron profile.

atoms, the experimentally extracted majority carrier profile will only match the dopant profile in regions where the carrier redistribution has a minimal impact, typically around 1×10^{16} to 1×10^{17} cm^{-3} or higher[27,28]. It is important to note that outside these resolution limits, we can certainly differentiate between a graded profile and a uniform dopant distribution. Figure 3b compares p(r)—experimental with p(r)—simulation starting with a flat dopant profile (N_a—flat), with the dopant concentration chosen to give the best fit to the experimental data. Even for this optimized dopant concentration, the agreement is much worse than with the simulated profile based on a diffusion model. Flat profiles at several other higher and lower dopant concentrations were not able to give a good fit to the experimentally extracted distribution, demonstrating that we can in fact distinguish between flat and graded dopant profiles. Additionally, the dopant profile extracted from a planar MOS structure processed similarly to the nanowire structure matches very well with the nanowire dopant profile, except towards the nanowire core (see Supplementary Information).

FEM three-dimensional simulations were used to generate an ideal C–V curve and compare it to the experimental C–V curve in order to determine the flat band voltage V_{fb} and further validate our dopant profiling and D_{it} extraction techniques. Figure 4 shows the FEM simulated C–V curves calculated from the diffusion and flat profiles shown in Fig. 3 compared with the high-frequency (20 kHz) experimental C–V curve (for the detailed procedure see Supplementary Information). Clearly, our experimental C–V curve does not match the flat dopant profile C–V curve, but is an excellent match to the simulated diffusion profile C–V. The only major deviation comes at full depletion, where the simulation goes essentially to 0 fF but the experimental curve saturates at 0.5 fF. This extra capacitance in the experiment may come from direct coupling between the surround gate and the nanowire leads; the simulation would not see this because it does not incorporate a back-gate and thus allows for the leads to become depleted. Because the simulation did not account for interfacial defects, the minor deviation in slope likely stems from interface states, which are known to cause stretch-out even in high-frequency C–V measurements (see Supplementary Information)[9]. The experimental C_{ox} of 2.58 fF, taken from the strong accumulation region of the 20 kHz C–V, is within 2.6% of the simulated C_{ox} value, using an Al_2O_3 dielectric constant of 7.3 for the full 15 nm of amorphous oxide measured in TEM and SEM. This excellent agreement further corroborates our dopant profiling and extraction method. The estimated fixed oxide charge value of -4.6×10^{11} cm^{-2} is also similar to previous literature reports for ALD Al_2O_3 on silicon (see Supplementary Information)[21].

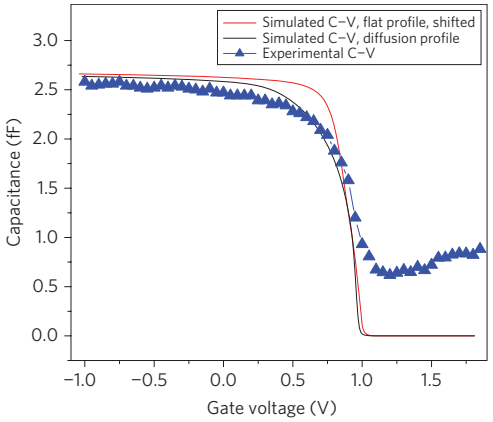

Figure 4 | Capacitance–voltage simulations. Experimental high-frequency 20 kHz C–V curve (blue) compared to the finite-element modelling (FEM) simulated C–V curves for the boron diffusion profile (black) and the flat profile (red) as shown in Fig. 3a and b, respectively.

In conclusion, we have measured silicon nanowire C–V curves at frequencies between 200 Hz and 20 kHz to demonstrate that the D_{it} profile as a function of position in the bandgap is qualitatively and quantitatively similar to results from bulk silicon with a peak of 1×10^{13} cm^{-2} eV^{-1} several hundred meV from the valence band edge and a mid-gap density near 4×10^{11} cm^{-2} eV^{-1}. This suggests it should be possible to obtain high-quality SiO_2/Si interfaces in nanowires comparable to those in bulk silicon under the proper thermal oxidation conditions, which will be critical for achieving high-performance electronic devices. The radial boron doping profile was also measured using the high-frequency C–V curve and matched the expected profile from dopant diffusion simulations with a surface concentration near the boron solid solubility of 1×10^{19} cm^{-3} and a sharp decrease down to around 1×10^{17} cm^{-3} towards the core. A flat dopant profile, such as is normally assumed using the standard method of estimating the doping level from the measured conductivity, mobility and threshold voltage cannot provide an accurate doping picture for our nanowires. These results unambiguously demonstrate that quantitatively understanding and controlling the surface properties and dopant distribution within semiconductor nanowires will be critical to achieve reproducible high-performance devices.

Methods

Device fabrication. Silicon nanowires were grown in a home-built CVD reactor at 830 °C with 10% H_2/Ar serving as both the diluent and carrier gas with flow rates of

158 and 50 s.c.c.m., respectively. The carrier gas was bubbled through liquid $SiCl_4$ chilled to 0 °C in order to maintain a constant vapour pressure. The photolithography patterned SOI trench substrates were sensitized with a 10% aminopropyltriethoxysilane in ethanol solution and then coated with 80-nm-diameter gold nanoparticles (Ted Pella) by means of drop-casting. The nanowires were boron doped by annealing for 1 h at 675 °C with 500 s.c.c.m. carrier gas and 0.5 s.c.c.m. 1% BCl_3/Ar, followed by 15 min at the same temperature with the BCl_3 line turned off. The Al_2O_3 gate dielectric was deposited in a home-built ALD chamber using alternating pulses of trimethylaluminium and water precursors. The surround gate metal was patterned by means of photolithography and chromium sputtering.

Capacitance measurements. Devices were contacted by wire-bonding from a pin package to the degenerately doped (boron) silicon source and drain pads and the chromium surround gate. Controls with two wire-bonds to the same silicon pad showed that there was no problem breaking through the Al_2O_3 and that the series resistance from the contacts or pads was negligible compared to that of the nanowires. For the C–V measurements, the source and drain were grounded and the bias voltages were applied to the surround gate and back-gate. The capacitance was measured between the surround gate and source–drain pads using an Andeen-Hagerling AH2700A ultra-precision capacitance bridge with an excitation amplitude of 20 mV and a scan rate low enough to minimize the noise at each frequency. For all the C–V curves reported here, the bias voltage was scanned from accumulation to depletion, but C–V curves scanned in the opposite direction were nearly the same due to the small hysteresis (see Supplementary Information). The entire sample was immersed in liquid nitrogen to maintain a constant temperature of 77 K.

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