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SUPPLEMENTARY INFORMATION

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Dopant profiling and surface analysis of silicon nanowires using capacitance-voltage measurements

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Dopant diffusion simulation

The expected radial dopant profile was simulated using TSupreme for boron in silicon with the PDFull model, which includes point defect and interstitial diffusion contributions (N_a – diffusion in Fig 4). The temperature, time and nanowire geometry were taken from the experimental doping conditions.

Interface state density calculation

For the measured C-V curves, there is significant frequency dispersion in the depletion region leading to a substantial shift between the high and low frequency curves. The increased low frequency capacitance in the depletion region is typically attributed to interface states that cannot respond quickly enough to the high frequency AC voltage signal and thus freeze out at increased frequencies. These states have some dispersion within the semiconductor band gap, so as the gate voltage causes the Fermi level to scan from the valence band edge to the center of the band gap (accumulation through depletion to onset of inversion) they can be populated or depopulated, depending on whether they are acceptor or donor type states. This change in charge will lead to an interface state capacitance (C_{it}) which can be converted to an interface state density (D_{it}) by dividing by the elemental charge and the interfacial area. D_{it} is extracted by creating an equivalent circuit diagram for the low and high frequency capacitance, C_{LF} and C_{HF} respectively and the result, known as the high-low method, is given by:

$$D_{it} = \frac{(C_{LF} - C_{HF})}{q\left(1 - \frac{C_{LF}}{C_{ox}}\right)\left(1 - \frac{C_{HF}}{C_{ox}}\right)2\pi r L} \quad \text{states cm}^{-2}\ \text{eV}^{-1} \qquad (1)$$

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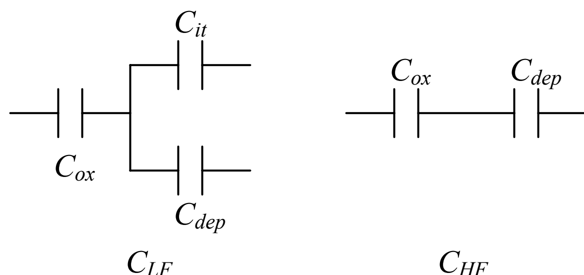

This gives D_{it} as a function of gate bias; to convert gate bias to position in the band gap, we compare the experimental C-V curve to the curve calculated with FEM using the simulated dopant diffusion profile (described below). The voltage offset gives the change in flat-band voltage (ΔV_{fb}, described below) which allows gate bias correlation between the theoretical and experimental C-V curves and then the band-bending can be mapped out versus gate bias with the FEM simulation. The gap energy with respect to the valence band is simply the band bending added to the flat-band Fermi level (i.e. the Fermi level calculated from the nanowire doping level).

Dopant profiling

Capacitance can be generally defined by:

$$C = \frac{dQ}{dV}$$

where C is the capacitance, Q is the charge on the capacitor and V is the voltage across the capacitor. Due to the cylindrical symmetry, the nanowire is depleted radially starting at the semiconductor surface as the surround gate bias scans from negative to positive values (p-type). Therefore, if we integrate the C-V curve from $V = V_1$ to $V = V_2$ we will get the charge located in the volume of silicon depleted over the same voltage change. This volume can be calculated using the total capacitance at each given gate bias by assuming that the depletion region acts as another cylindrical insulator in series with the gate oxide. The total (measured) capacitance is then given by:

$$C = \frac{C_{dep} C_{ox}}{C_{dep} + C_{ox}}$$

Since we measure the oxide capacitance in the accumulation region and total capacitance versus voltage, we can easily calculate the depletion layer capacitance at each voltage. Using the standard formula for capacitance of coaxial cylinders gives:

$$C_{dep} = \frac{2\pi\varepsilon\varepsilon_o}{\ln\left(\frac{r_2}{r_1}\right)}$$

where ε is the silicon dielectric constant, ε_o is the vacuum permittivity and r_1, r_2 are the inner and outer radii of the depletion region, respectively. Since r_2 is

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simply the nanowire radius for all voltages, we can calculate the inner edge (and thus the width) of the depletion region versus voltage to get the depletion volume at each voltage. If we assume that the charge in the semiconductor comes entirely from the majority carriers, then we can divide the charge (calculated by integrating the C-V curve as mentioned above) by the depletion volume to get the majority carrier concentration as a function of radius. Finally, we can correct for the slight perturbation in the C-V slope caused by interfacial states being populated/depopulated as we scan the gate bias (known as "stretch-out") by comparing the low and high frequency capacitance values, analogous to the D_{it} calculation described above:

$$N_a^*(r) = \frac{\left(1 - \frac{C_{LF}}{C_{ox}}\right)}{\left(1 - \frac{C_{HF}}{C_{ox}}\right)} N_a(r)$$

where $N_a(r)$ is the carrier profile extracted directly from the data and $N_a^*(r)$ is the profile corrected for stretch-out. As the interface state density goes to zero, C_{LF} and C_{HF} converge, so the correction factor falls out of the expression.

Simulated C-V curves

The nanowire transistor geometry taken from the experiment was input into the Comsol Multiphysics program, with the dopant distribution given by the simulated dopant diffusion profile (or several flat dopant distributions). The ends of the nanowire were grounded (V=0) and the gate voltage was scanned as in the experiment. The program numerically solves Poisson's equation to get the 3-D charge distribution as a function of voltage. The initial majority carrier distribution (p(r) – diffusion in Fig 4) therefore is simply the radial charge distribution at no applied bias. For a uniform dopant distribution p(r) is identical to the dopant concentration throughout the wire, but this is not the case for non-uniform dopant profiles as seen in Fig 4. The FEM simulations were performed and compared to the experimental results in the following way:

Generating C-V curves:

1. A 3-D model of a surround-gate nanowire with appropriate radius and oxide thickness was built. The nanowire length was scaled shorter than experiment to allow for reasonable computation times, but kept long enough to ensure no fringe capacitance or length effects.
2. The dopant profile of interest (e.g. diffusion or flat) was input into the nanowire.
3. The electrostatic finite-element simulation was run at various V_g, each time giving a net charge induced in the nanowire Q.
4. A *C-V* curve is then generated from this Q vs. V_g data by $C = dQ/dV_g$, which can be compared to experimental *C-V* curves as shown in Fig. 5.

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Calculating dopant profiles:
The simulated majority carrier profiles (e.g. Fig. 4) are calculated from the simulated C-V curves with the *exact* same method used to calculate experimental dopant profiles from experimental C-V curves as explained in the text. This dopant profile extraction method is based on the depletion approximation and thus leads to artifacts and inaccuracies in extracted dopant profiles (Fig. 4 blue squares and red circles). However, since we know the actual dopant profile in the simulation (Fig. 4 black line) we can find the actual profile that results in the best fit between the *extracted* simulation and experimental profiles. In this way, the FEM simulations allow us to find the radial dopant profile in our nanowires with minimal artifacts from electrostatic Debye Length limitations. In Fig. 4 of the text, we show that the diffusion profile (Fig. 4a) results in a much better fit to the experimental data than the best flat profile (Fig. 4b).

Fixed charge density calculation

The voltage shift between the experimental and simulated C-V curve, ΔV_{fb}, ideally is given by:

$$\Delta V_{fb} = (\phi_m - \phi_s) - \frac{(Q_{it} + Q_f)}{C_{ox}}$$

where $(\phi_m - \phi_s)$ is the metal-semiconductor work function difference, Q_{it} is the interfacial trap charge, Q_f is the fixed oxide charge and C_{ox} is the oxide capacitance (measured in the accumulation region) . Using the voltage shift of 0.05 V along with the Cr work function from literature, the calculated Si Fermi level from the doping level, and the measured oxide capacitance leads to a total interfacial charge value of $-7.9 \cdot 10^{-16}$ C. Normalizing by the device area and dividing by the electron charge gives a total charge state density of $9.1 \cdot 10^{11}$ cm^{-2}. Using the mid-gap D_{it} value calculated from the high-low method gives a fixed oxide charge density of about $4.6 \cdot 10^{11}$ cm^{-2} (assuming negative fixed oxide charge), consistent with literature reports for ALD Al_2O_3 on silicon from trimethylaluminum and water precursors.

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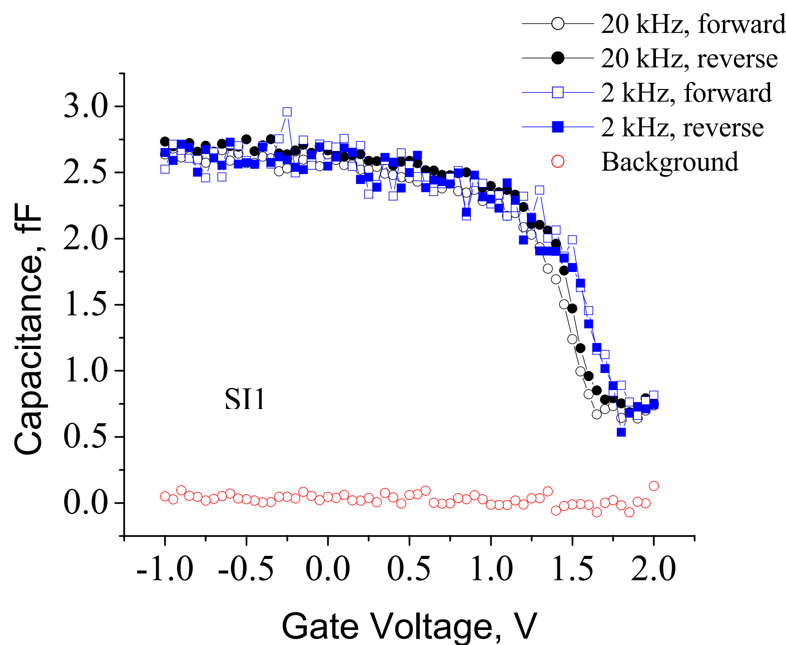
Hysteresis in C-V curve.

Figure SI1 shows that there is little hysteresis in the C-V curve. Both 2 kHz and 20 kHz curves are shown for both scan directions.



Planar Control MOS Capacitors

We also fabricated planar control MOS capacitors starting with p-Si (111) wafers with a doping level of about $1*10^{15}$ cm^{-3} (according to manufacturer) and using the same boron doping, ALD Al_2O_3 deposition and Cr gate metal deposition procedures as for the nanowire devices. The Cr gate pads were squares, 41 microns on an edge (measured by SEM) and the Al_2O_3 was 16 nm thick according to a Nanospec interferometer. C-V measurements were conducted using the same capacitance bridge as for the nanowire measurements but in a Janis ST-500 cryogenic probe station at 77K instead of wirebonded to a pin package (wirebonding shorted the planar devices). The measurement parameters were the same as for the nanowire devices (SI2). The dopant profile and interface state density distribution extracted from the planar devices match very well with those from the nanowire devices (SI3, SI4). The dopant profile extraction method was the same as for the nanowire (but using planar geometry instead of cylinder) and the profile was exactly the same as that extracted with the standard method for planar devices (slope of Mott-Schottky curve). The Al_2O_3 dielectric constant calculated from the oxide (accumulation region) capacitance was 6.8 for the nanowire devices and 7.0 for the planar devices. The mid-gap interface state density was about 3 times higher for the nanowire

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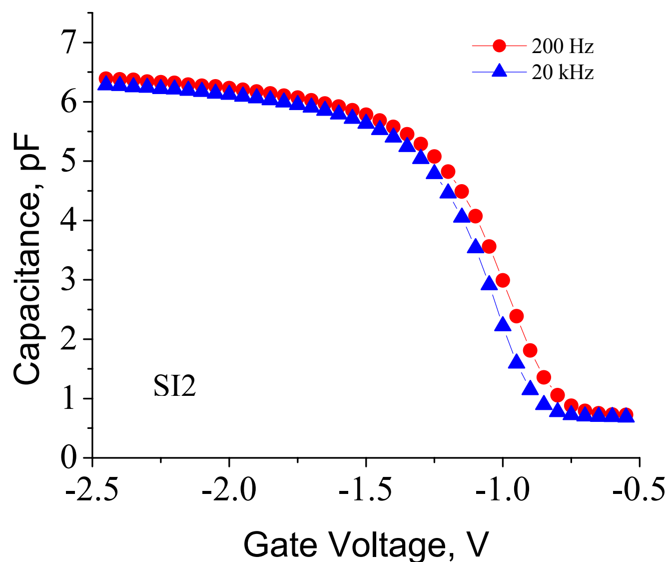
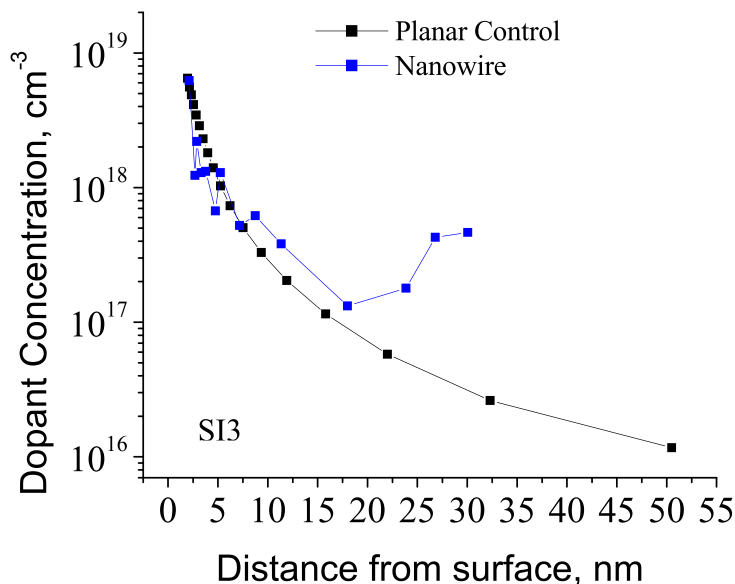
than for the planar control, which may be due to the difference in surface planes ({111} planes in the planar versus {211} planes on the nanowire); it is well known that interface state density can vary by as much as an order of magnitude for the same oxide deposition procedure on Si (100) vs. Si (111). We did not have Si (211) wafers to use as a comparison.





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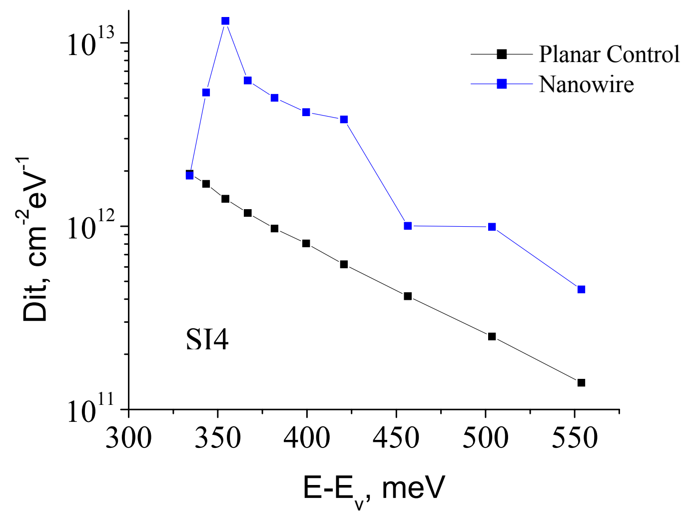

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