Supporting Information

Nanofluidic Diodes based on Nanotube Heterojunctions

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Heterojunction Nanotube Synthesis

Silicon nanowire arrays were prepared using chemical vapor deposition (CVD) epitaxial growth using silicon tetrachloride ($SiCl_4$, Aldrich, 99.99%) as the silicon source. Hydrogen (10% balanced by argon) is used to reduce $SiCl_4$ at high temperature (810-850˚C). Gold Nanoparticles (Ted Pella, Inc, 50nm) was deposited on Si (111) substrates to initiate the growth of epitaxial silicon nanowire array via the vapor-liquid-solid (VLS) growth mechanism. The vertical silicon nanowire array was first coated with Al_2O_3 by Atomic Layer Deposition (ALD) at 200˚C in a flow reactor. ALD is a film deposition technique that produces highly conformal, uniform and controlled thin films. Precursor gases for the Al_2O_3 deposition, $Al(CH_3)$ (trimethylaliuminum [TMA]) and H_2O are alternately pulsed into the reactor and then purged away, resulting in a self-limiting growth process that constructs a film one monolayer at a time. The growth rate at 200˚C in the ALD reactor used is calibrated to be 1.2Å/cycle, so 250 cycles are deposited to yield a 30nm Al_2O_3 film on the SiNWs.

PMMA (polymethyl methacrylate, M.W. 35k, 5% in Ethanol) solution was then drop-casted on the SiNW array as a mask to protect the bottom half of SiNWs from subsequent etching. The thickness of the PMMA mask was controlled by oxygen plasma etching till 2/5 of the total length of the SiNWs are exposed. The substrate was then etched in 1:5 Buffered Hydrofluoric Acid (BHF) bath to remove the Al_2O_3 coating on the exposed part of the array. The etching process was monitored with SEM to make sure of the complete

removal of the oxide layer on the top half of the SiNWs. After etching, the PMMA mask was removed with CH_2Cl_2 and the substrate was then re-coated with SiO_2 by RF Plasma Sputtering. Finally, the core-shell nanowires were broke off from the substrate and transferred to a fused silica substrate/or a TEM grid. The substrate with the core-shell nanowires were then loaded into a Xetch® Xenon Difluoride Etching System to etch away the Si cores and release Al_2O_3/SiO_2 di-block nanotubes. XeF_2 etching is an all gas phase, room-temperature, isotropic silicon etching process that has very high selectivity to many oxides thin films including SiO_2 and Al_2O_3 (~2000:1). It thoroughly removed the Si nanowire template while leaving the oxide coating intact and the inner surface of the resultant nanotubes smooth.

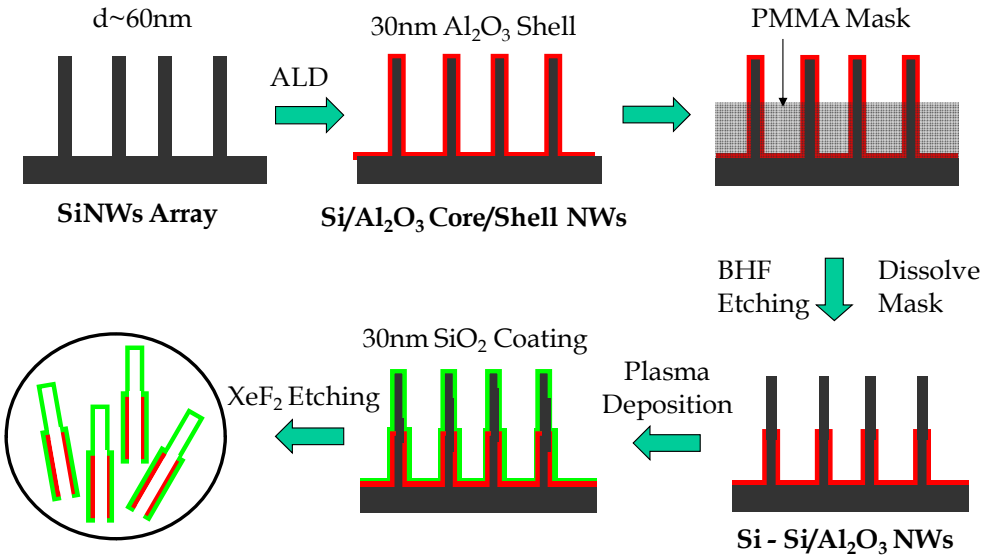

Figure S1. Process flow for the fabrication of SiO_2-Al_2O_3 Diode Nanotube Array

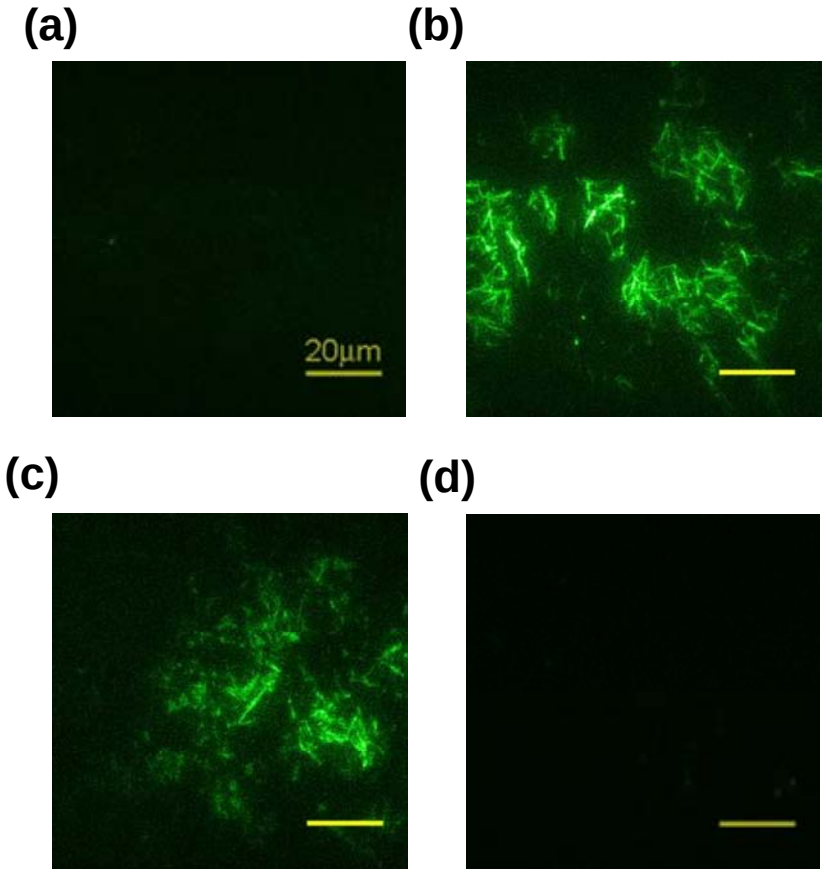

Figure S2 Fluorescent micrographs of dye-loaded pure SiO_2 and Al_2O_3 nanotubes under 442nm laser excitation. **a**. Pure SiO_2 tube loaded with Fluorescein. **b**. Pure SiO_2 tube loaded with R6G. **c**. Pure Al_2O_3 tube loaded with Fluorescein. **d**. Pure Al_2O_3 tube loaded with R6G.

Nanotube diode device fabrication

Nanofluidic diode devices interfaced with microfluidic channels (Figure 4a) were fabricated using a modified procedure. Si nanowires, which will later template the diode nanochannel, were grown laterally from the side wall of microtrenches that were prefabricated on silicon-on-insulator (SOI) wafer according to a well-established procedure developed in our group (Figure S3-a). The whole substrate was then coated with 30nm conformal Al_2O_3 layer by ALD (Fig S3-b). Photoresist were patterned by photolithography to protect

the Al_2O_3 coating on one half of the microtrenches and any bridging nanowire (Fig S3-c,d) while the Al_2O_3 layer on the rest of the substrate was removed by BHF etching (Fig S3-e). After dissolving the photoresist mask, SiO_2 were deposited on the substrate with RF plasma sputtering (Fig S3-f). The substrate was then put on a glass slide and packaged in polydimethylsiloxane (PDMS) (Fig S3-g). Holes were then opened on top of the Si pads on both sides of the microtrenches that have bridging nanowires (Fig S3-h). The top oxide directly beneath the holes was removed by CF_4 anisotropic Reactive Ion Etching (Plasma-Thermal Parallel Plate Plasma Etcher). And the substrate was immediately loaded into XeF_2 etching chamber to remove the Si pads and nanowires and open SiO_2 microfluidic channels and diode nanofluidic channels. Ag/AgCl electrodes were used in the microfluidic channels on either side of the nanofluidic channels for applying electrical bias (Fig S3-i). SEM images of a single bridging SiNW at different stage of fabrication was given in Fig S4 (a)-(c). Fig 4b is an optical image showing the structure of the final diode device while it was being filled by Deionized water.

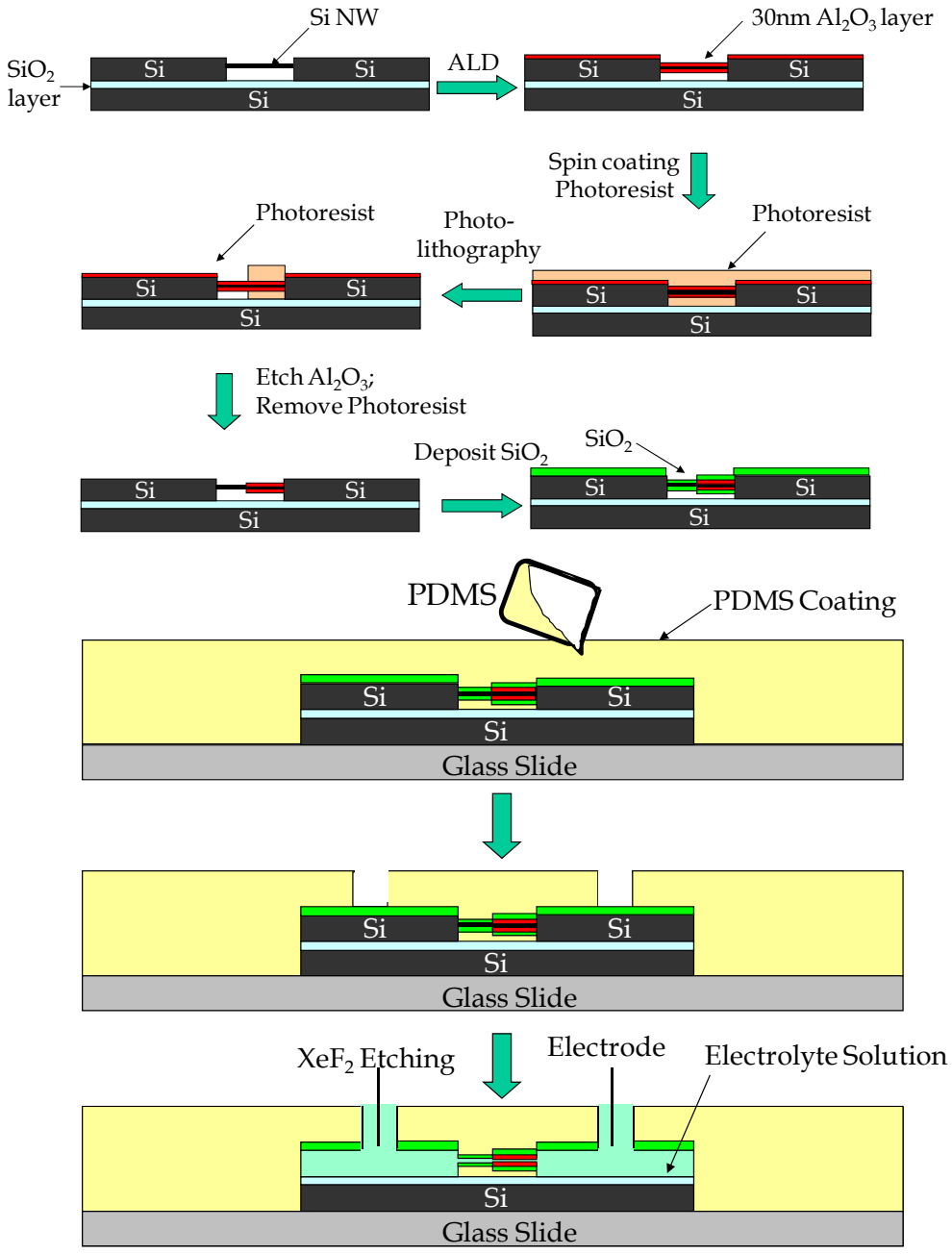

Figure S3 Process flow for the fabrication of SiO_2-Al_2O_3 diode device.

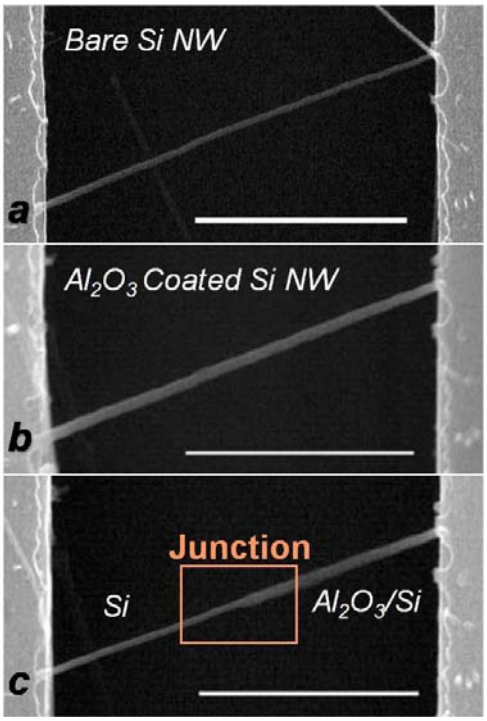

Figure S4 SEM images of a Si nanowire bridging the side walls of a 5μm microtrench at different stage of nanotube diode device frabrication. **a**. As-grown SiNW. **b**. The SiNW coated with a 30nm ALD Al_2O_3 layer. **c**. The Si-Al_2O_3/Si junction formed after removing photoresist mask and etching in BHF solution.

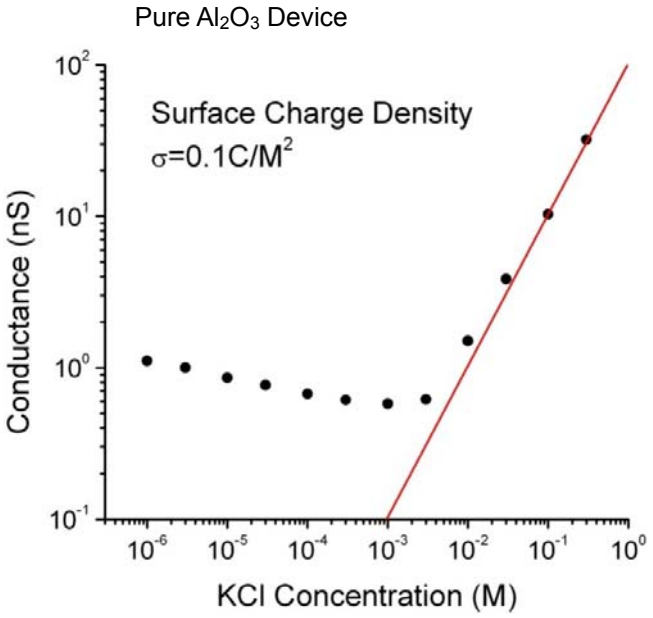

Figure S5 The electrical conductance of the pure Al_2O_3 nanotube device. The measured surface charge density of pure Al_2O_3 nanotube was ~0.1C/m^2, comparable to pure SiO_2 nanochanels reported previously (0.01-0.1C/m^2).

Figure S5 shows the measured ionic conductance of pure Al_2O_3 nanotube devices measured at different concentration of KCl solution under low bias voltage. It shows unipolar characteristics that deviates from the bulk behavior at low concentration, which confirm surface-charge governed transport, in consistent with the SiO_2 nanotube devices reported previously. The surface charge density can be estimated from the ionic current in the unipolar transport region.

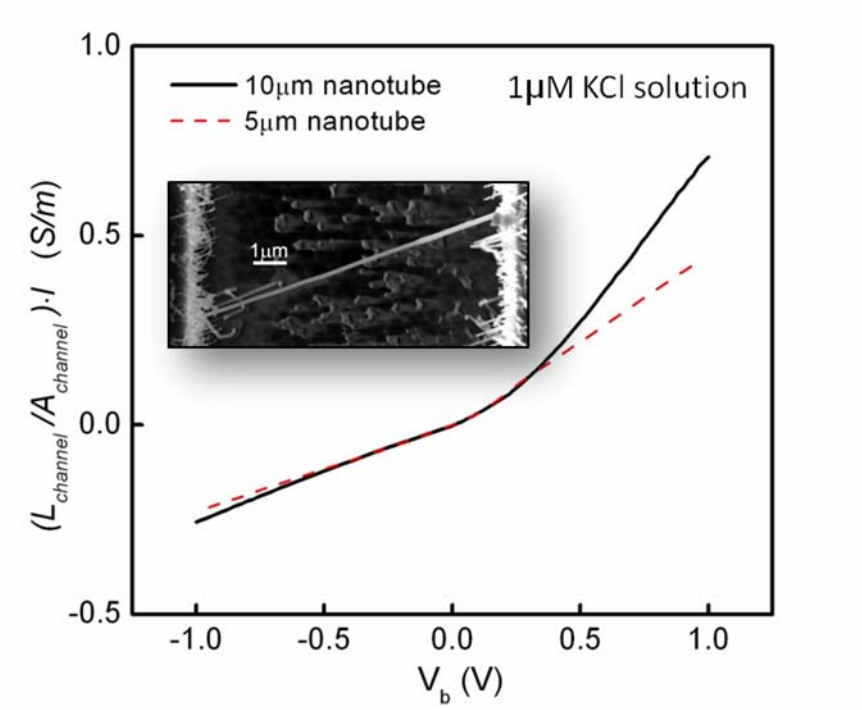

Figure S6 The dependence of diode rectification on the length of the nanochannel. The ionic current of a 10μm nanotube diode device normalized to the channel dimension $(L_{channel}/A_{channel})\cdot I$, where I is ionic current measured under bias voltage V_b, $L_{channel}$ is the length of the PN nanochannel and $A_{channel}$ is the area of PN nanochannel cross section, shows a significant increase compared to a typical 5μm nanotube diode device at unipolar concentration region. Inset: SEM images of the 10μm long Si- Al_2O_3/Si nanowire, which was later made into the 10μm nanotube diode device measured.

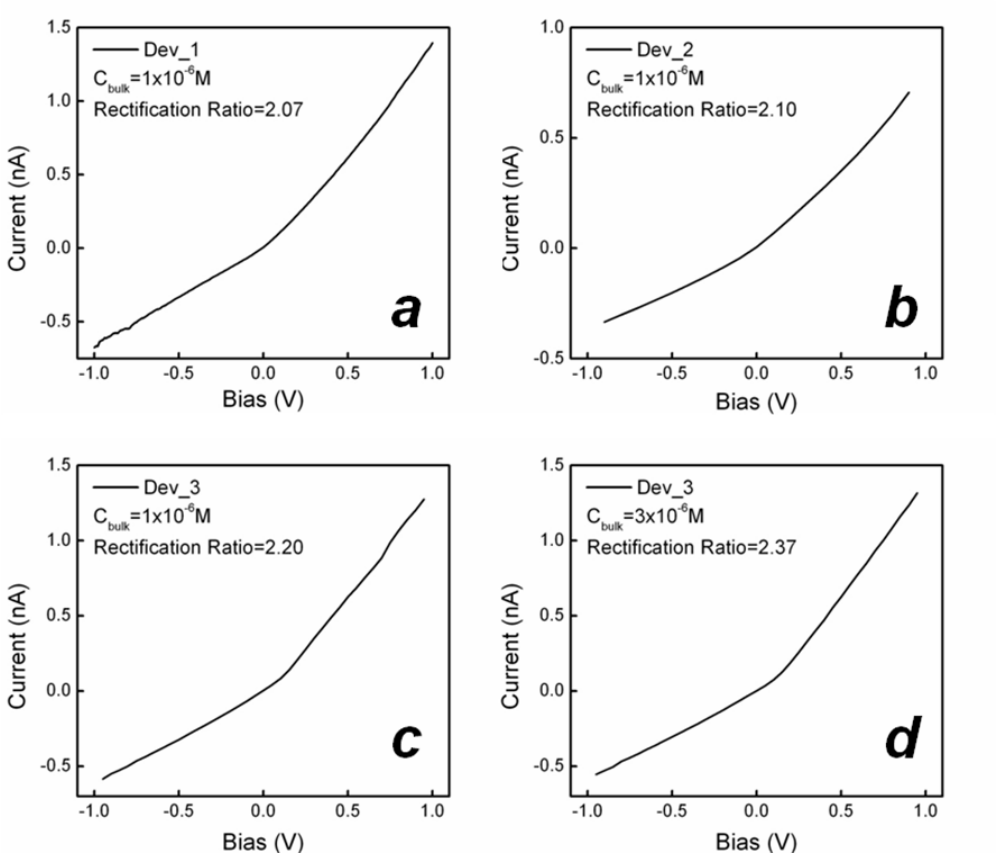

Figure S7 Device reproducibility. (a-c) I-V curve of three different nanotube diode devices at 1μM bulk KCl concentration. Current rectification ratios are consistent among devices. (d) I-V curve of Dev_3 at 3μM bulk KCl, consistent with the rectification ratio reported in Figure 4.