

# Single Crystalline Mesoporous Silicon Nanowires

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## ABSTRACT

Herein we demonstrate a novel electroless etching synthesis of monolithic, single-crystalline, mesoporous silicon nanowire arrays with a high surface area and luminescent properties consistent with conventional porous silicon materials. These porous nanowires also retain the crystallographic orientation of the wafer from which they are etched. Electron microscopy and diffraction confirm their single-crystallinity and reveal the silicon surrounding the pores is as thin as several nanometers. Confocal fluorescence microscopy showed that the photoluminescence (PL) of these arrays emanate from the nanowires themselves, and their PL spectrum suggests that these arrays may be useful as photocatalytic substrates or active components of nanoscale optoelectronic devices.

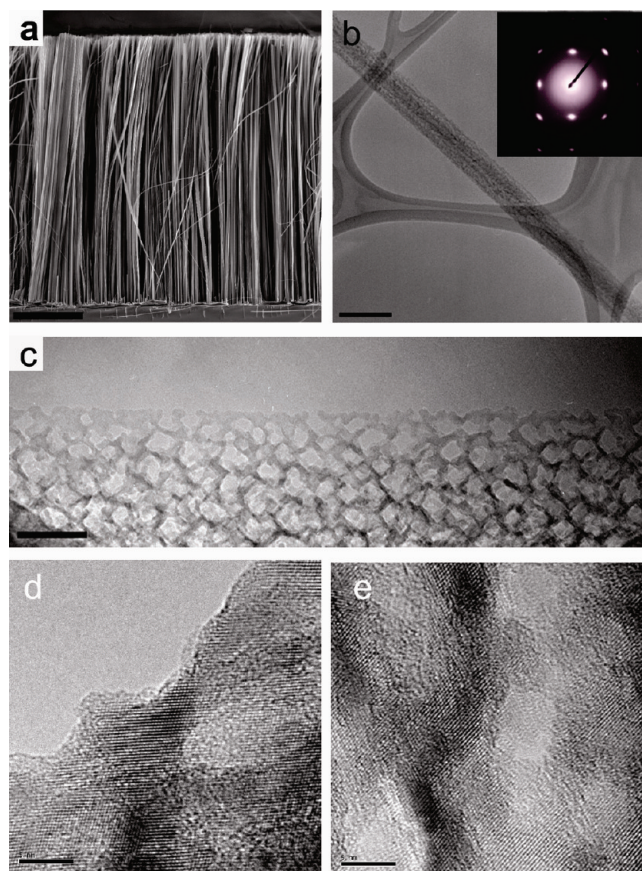
Porous semiconductors have garnered significant attention for their novel chemistry and potential applications as high surface area and optically active substrates.<sup>1–5</sup> Porous silicon in particular has long been studied for its potential applications in optoelectronics and sensing as a result of its light-emitting properties.<sup>6–10</sup> In addition, they can also serve as a drug or gene delivery matrix because of their good biocompatibility.<sup>11,12</sup> Porous silicon is typically synthesized by applying a voltage bias to a silicon substrate immersed in an aqueous or ethanoic hydrofluoric acid (HF) solution. Surface and charge instabilities at the solid–solution interface are thought to nucleate pore formation, and accelerated etching of silicon at the pore tips propagates the voids into the substrate. The resulting pore networks and remaining silicon scaffold form the structure of porous silicon.<sup>13,14</sup> The synthetic method described in this study, on the other hand, relies on an electroless metal deposition process to provide the current flux necessary for porous silicon formation. Electroless metal deposition and subsequent sacrificial etching of the surrounding silicon lattice has been previously observed<sup>15</sup> and exploited to controllably etch arrays of silicon nanowires.<sup>16</sup> We have now found that it is possible to etch arrays of single-crystalline mesoporous silicon nanowires without the application of an external voltage.

Silicon wafer pieces (boron-doped, of various resistivities) were cleaned by sonication first in acetone and then isopropyl alcohol. Immediately before immersion in the etching solution, the substrates were also soaked in diluted hydrofluoric acid (HF 10:1). The etching bath comprised an aqueous solution of 0.01–0.04 M AgNO<sub>3</sub> and 5 M HF, and the wafer was left to soak for 3–4 h at 25–50 °C. Upon removal from

the etch bath, the loose film of dendritic Ag deposited on the top surface of the nanowires arrays was washed off by spraying with deionized water. The remaining Ag was dissolved by dipping the wafer pieces in concentrated nitric acid. The resulting arrays were vertically oriented and comprised single crystalline nanowires covering approximately 40% of the wafer area.

Not all types of silicon wafers produced nanowires with identical texturing. As previously observed,<sup>17</sup> the surface roughness of the nanowires increased—as gauged by transmission electron microscopy (TEM)—with decreasing resistivity of the original wafer. At the extreme, silicon p-type wafers with a resistivity less than 5 mΩ·cm produced porous nanowires. The progression of surface roughness and the evolution of porous structures with decreasing wafer resistivity can be seen in the TEM micrographs in Figure 1 and Figure S1 (Supporting Information), corresponding to wafer resistivities of 10000, 10, and <5 mΩ·cm, respectively.

As grown, the arrays of porous nanowires appear similar to those etched from more resistive wafers. The nanowires were vertically oriented, as seen in Figure 1a, and selected area electron diffraction (SAED) patterns obtained from them by TEM showed they were single crystalline, as seen in the typical pattern in Figure 1b (inset). The diffraction spots in the SAED pattern are smeared into small arcs. This stretching of the diffraction intensity about the intensity peaks is probably a result of significant strain present within the crystal: the thin regions of crystalline silicon contort slightly due to tension at the interface with the native oxide. The single-crystalline nature of the nanowires is further indicated by the silicon lattice which can be clearly seen in the high-



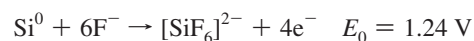
**Figure 1.** Structural characterization of electrolessly etched porous silicon nanowires. (a) A cross-sectional SEM of the porous nanowire array. The nanowires are vertically oriented and part of a monolithic silicon crystal including the remaining wafer from which they were etched ( $<0.005 \Omega\text{-cm}$  wafers). (b, c) TEM micrographs of the porous nanowire from which the SAED (panel b inset) pattern was obtained. The diffraction pattern indicates the nanowire is single crystalline. (d and e) Phase contrast TEM images of the silicon lattice surrounding pores near the surface and in the interior of the nanowire, respectively. Note that the crystal lattice is as thin as several nanometers at points and is continuous around the pores. Scale bars are  $10 \mu\text{m}$ ,  $200 \text{ nm}$ ,  $50 \text{ nm}$ ,  $5 \text{ nm}$  and  $5 \text{ nm}$ , respectively.

resolution TEM (phase contrast) images of the surface and interior of a porous silicon nanowire in panels d and e of Figure 1, respectively. Though difficult to directly observe by TEM, since the observed image is a two-dimensional projection of the nanowire, panels d and e of Figure 1 show several pores around which the silicon lattice is continuous. The diameter of the pores appears to be approximately  $10 \text{ nm}$ , and the remaining silicon scaffolding is as thin as several nanometers at points. The TEM micrograph in Figure 1c shows a nanowire that has been immersed in diluted HF for  $2 \text{ min}$  to remove the native oxide. The resulting square structure and faceting of the pores indicates that the pore etching occurs along specific crystallographic directions. In addition, X-ray diffraction data collected on these porous silicon nanowires exhibited characteristic diffraction peak broadening as a result of nanoscale crystalline silicon domains (Figure S2 in Supporting Information).

Though electroless synthesis of porous silicon has not been previously observed, it likely proceeds by a similar electro-

chemical mechanism to conventional porous silicon. The main difference between this and previous porous silicon syntheses is that the current flux used here to induce porosity is provided by continuous  $\text{Ag}^+$  reduction from solution rather than an applied bias through electrical contacts. As previously described,<sup>15,16,18</sup> reduction of metal atop the wafer oxidizes the silicon immediately surrounding nanometer-scale metal deposits on the wafer surface. This silicon dissolves in the HF solution and the metal particles etch pits down into the wafer, leaving behind the nanometer-scale pit walls between the particles which form the resulting nanowires.

During the wafer etching process, there is a simultaneous electrochemical reaction responsible for etching the nanowire surface leading to varying degrees of surface roughness and porosity. The electrochemical cell is composed of the Ag deposits as the active cathode upon which more  $\text{Ag}^+$  reduces, and the silicon nanowires as the anode, from the surface of which silicon dissolves into aqueous HF solution. The half-cell reactions are as follows



The oxidation and dissolution of silicon injects electrons into the cathode upon which  $\text{Ag}^+$  reduces, thus generating a standard reduction potential of  $2.04 \text{ V}$  (vs SHE). This current flow induces etching at the nanowire surface surrounding the Ag just as an electrical bias induces etching of a silicon wafer surface in an aqueous solution containing only HF (no  $\text{Ag}^+$ ).

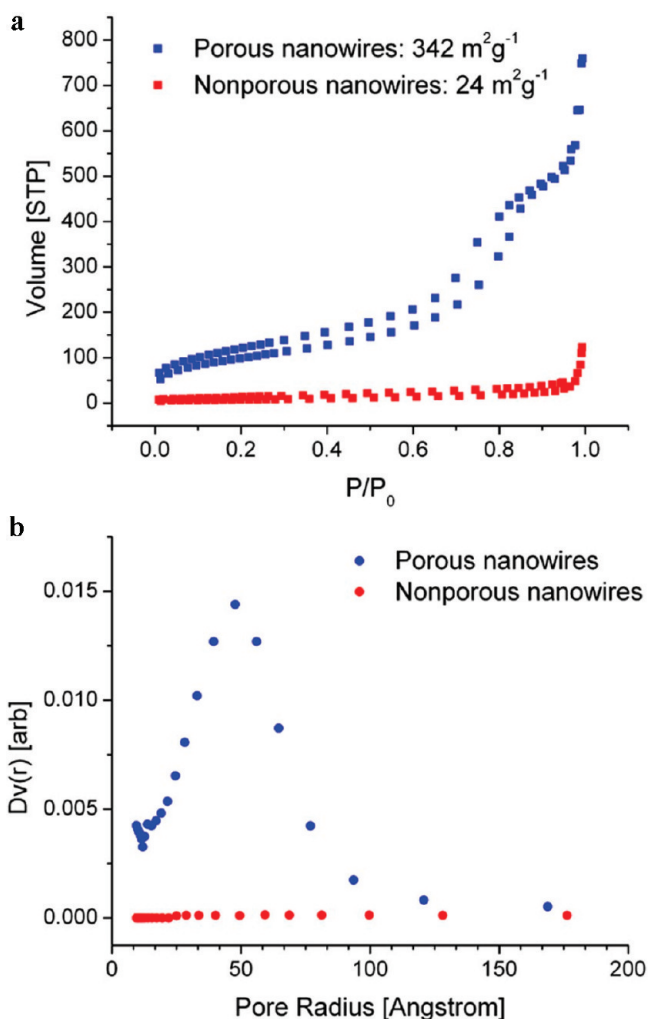
The observed increase in surface roughness and porosity with decreasing resistivity can be a result of one or both of the following factors. First, lower resistivity wafers have higher dopant atom concentrations. In some models of the mechanism for porous silicon formation, crystal defects and impurities at the silicon surface are thought to serve as nucleation sites for pore formation.<sup>14</sup> As a result, higher dopant concentrations may create a larger thermodynamic driving force for pore formation, or at least increase the rate of etching and surface roughness. Second, higher dopant concentrations lower the energy barrier to charge injection across the silicon surface, thus increasing current flow under the same applied bias. The silicon electronic bands equilibrate upon contact with the solution forming an energetic (Schottky) barrier that inhibits charge transfer across the interface.<sup>19</sup> The bands, pinned at the interface, bend to equalize the Fermi energy of the silicon and the equilibrium redox potential of  $\text{Ag}^+/\text{Ag}^0$ . Since the redox potential of  $\text{Ag}^+/\text{Ag}^0$  lies below the valence band of silicon,<sup>20</sup> higher p-type dopant concentrations (i.e., lower Fermi level) will cause the bands to bend less and decrease the depletion width and potential,  $\phi_{\text{sc}}$ , of the energy barrier at the surface,  $e\phi_{\text{sc}}$ . Under the same cell potential a lower barrier will increase charge flow, thus increasing roughness or porosity as is the case with porous silicon etched under an applied bias.<sup>21</sup> Correspondingly, n-type wafers produced

only rough nanowires without pores, regardless of the dopant concentration.

Surface area measurements were conducted according to the Brunauer–Emmett–Teller (BET) gas (nitrogen) adsorption method.<sup>22</sup> To collect enough material (approximately 15–20 mg) such that mass determination contributed negligible error to the final surface area measurement, nearly half a 4 in. wafer was used to generate nanowire arrays. After the standard synthetic procedure described above was followed, the porous nanowires were removed from the intact wafer by scraping with a razor blade. The resulting powder was poured into the sample cell and degassed overnight at 250 °C before determining the mass of the material, which was also confirmed by weighing after the surface area measurements. The adsorption/desorption isotherms were measured using a Quantachrome Autosorb-1 instrument and analyzed with Autosorb1 software. Porous nanowire arrays were etched from wafers with a resistivity <math><0.005 \text{ } \Omega\cdot\text{cm}</math> while nonporous control samples, with little surface roughness as indicated by TEM imaging, were etched under the same reaction conditions from approximately 10  $\Omega\cdot\text{cm}$  wafers. The TEM images of the porous and nonporous samples correspond to those shown in Figure 1 and Figure S1 in Supporting Information, respectively.

Standard BET analysis of nitrogen adsorption isotherms of the porous nanowires shows that the arrays of single crystalline nanowires have exceptionally high surface areas. Typical adsorption/desorption isotherms for both the nonporous control and porous nanowire powders are shown in Figure 2a. Multipoint BET analysis of multiple adsorption isotherms yields a mean surface area of 342  $\text{m}^2\cdot\text{g}^{-1}$  and a total pore volume of 0.88  $\text{cm}^3\cdot\text{g}^{-1}$  for the porous nanowires. For the purposes of comparison, this surface area corresponds to an equivalent area of 490  $\text{m}^2\cdot\text{g}^{-1}$  for porous silica due to the difference in density. The nonporous control nanowires have a surface area of only 24  $\text{m}^2\cdot\text{g}^{-1}$ , likely due to adsorption on the surfaces of the nanowires only. The BET surface area of the porous nanowires is remarkably high for a continuous single crystalline material and is comparable to that of the highest values for microporous silicon,<sup>23</sup> the structure of which is not necessarily single crystalline, and even mesoporous silica ( $\sim 1000 \text{ m}^2\cdot\text{g}^{-1}$ ).

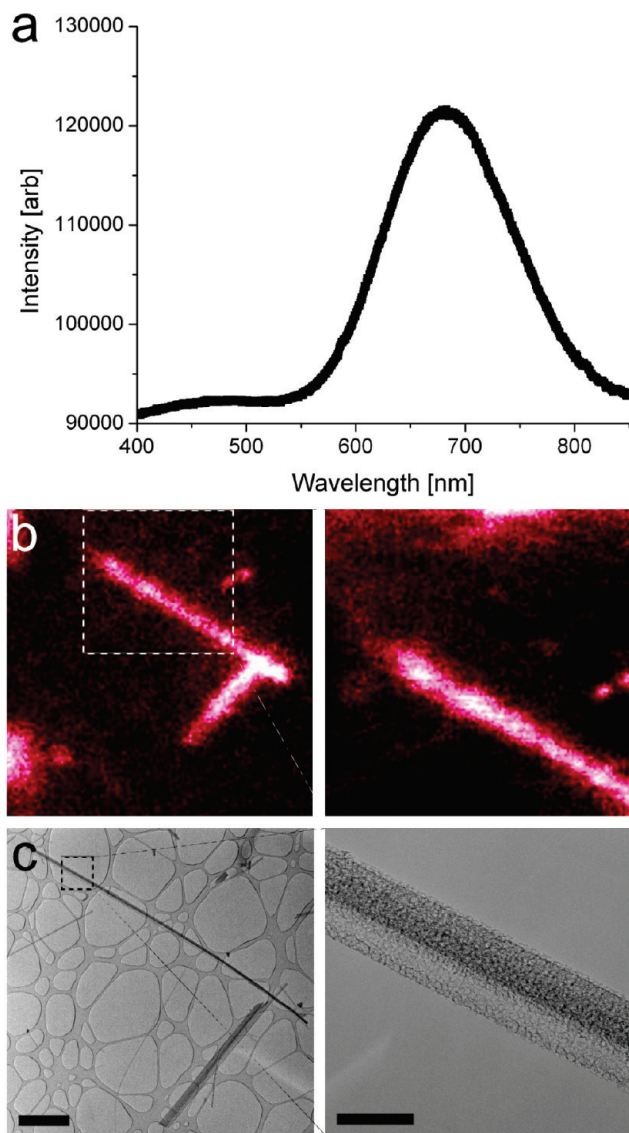
Determination of the pore radius distribution from the nitrogen adsorption isotherm using the Barret–Joyner–Halenda model suggests that the porous silicon wires are indeed mesoporous. Typical pore radius distributions for the porous and nonporous nanowires are shown in Figure 2b. As expected, the distribution for the control sample is flat across all radii due to the lack of pores, confirming observations from TEM imaging, and the only nitrogen adsorption occurs on the nanowire surfaces and between nanowires in bundles. The porous nanowires, on the other hand, have a wide pore size distribution lying squarely within the mesoporous regime. The nanowire pores range from approximately 2 to 20 nm in diameter, with a mean pore diameter of 9.7 nm. These values are consistent with estimates from TEM analysis, and the broad range of



**Figure 2.** Nitrogen adsorption measurements of mesoporous nanowires. (a) Typical nitrogen adsorption isotherms of mesoporous and nonporous nanowire samples (blue and red squares, respectively). The mesoporous nanowires were etched from low resistivity silicon wafers whereas the nonporous nanowires were etched from highly resistive wafers. The mean BET surface areas of the mesoporous and nonporous samples are 342 and 24  $\text{m}^2\cdot\text{g}^{-1}$ , respectively. (b) Typical BJH pore size distributions for mesoporous and nonporous nanowire samples (blue and red circles, respectively). The distributions confirm observations from TEM imaging of pore structures and the lack thereof in the two nanowire samples. The mean pore diameter of the mesoporous nanowires is 9.7 nm.

diameters is attributable to the random distribution of pore etching rates as a result of the galvanic displacement process.

The shape of the adsorption isotherm in Figure 2a of the porous nanowires is a clear example of a type IV isotherm characteristic of mesoporous materials. The steplike plateau indicating capillary condensation occurs at  $P/P_0 \sim 0.8$ . The persistent hysteresis over a wide  $P/P_0$  range below the condensation step probably results from the relatively large average pore diameter and condensation between nanowires in bundles, which are prevalent in the as-grown nanowire arrays.<sup>22,24</sup> The high surface area, mesoporous structure, and large pore volume indicate that these silicon nanowires will be an interesting porous semiconductor system for further study and application.



**Figure 3.** Photoluminescence of mesoporous nanowires. (a) Typical photoluminescence spectrum from mesoporous nanowires on a silicon wafer. (b) Confocal photoluminescence images from an assembly of mesoporous nanowires on a TEM grid. (c) TEM micrographs of the same wires, showing consistent porosity and microstructure along their lengths. Scale bars are 2  $\mu\text{m}$  and 200 nm, respectively.

Given the thin diameter of the crystalline silicon scaffold remaining after electroless etching, one would expect this material to photoluminesce much like the nanocrystalline nodes of porous silicon.<sup>3,14</sup> Indeed, under irradiation with 442 nm light from a HeCd laser, the mesoporous silicon nanowires emit visible light. To verify that the light originated from the mesoporous nanowires they were scratched from the growth substrate and transferred to a polished, clean silicon wafer. As shown in Figure 3a, the emission spectrum is broad—approximately 140 nm full width at half-maximum—and centered at 680 nm. The light emitted from the arrays upon laser irradiation is visible to the naked eye and appears orange to red in color. Wires were also dispersed on TEM grids and imaged by scanning confocal photoluminescence microscopy. Isolated wires were photoexcited by the focused beam spot of the HeCd laser,

which was scanned across the grid to generate an intensity map of the fluorescence from the nanowire. The intensity of light emission is consistent along the length of the nanowires, and TEM imaging (Figure 3c) confirmed the continuity of the nanowire microstructure. While we cannot exclude the possibility of emission from surface/defect states in surface oxide, photoluminescence at these wavelengths is consistent with silicon nanoparticles 3–4 nm in diameter, meaning excitons generated within the mesoporous silicon nanowire array could be energetic enough to drive pertinent photoelectrochemical reactions.<sup>10</sup>

In summary, we have elucidated a new electroless synthesis for single-crystalline mesoporous silicon nanowire. The resulting nanowire arrays possess a high surface area and optical properties characteristic of conventional porous silicon. The photoluminescence of these nanowires suggests they are composed of crystalline silicon with small enough dimensions such that these arrays may be useful as photocatalytic substrates or active components of nanoscale optoelectronic devices. Furthermore, this synthesis defines a novel route to electroless etching of mesoporous semiconductors and, with further understanding of the underlying chemical mechanisms, may be applied to other low band gap semiconductor systems.

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**Supporting Information Available:** Figures showing TEM micrographs of silicon nanowires etched from wafers and XRD patterns for porous Si nanowires collected in powder form. This material is available free of charge via the Internet at <http://pubs.acs.org>.

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