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FRONTIERS ARTICLE

Efficiency enhancement of copper contaminated radial p–n junction solar cells

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ABSTRACT

Radial p–n junction solar cells have been predicted theoretically to have better efficiencies than their planar counterparts due to a decrease in the distance required to collect minority carriers relative to carrier diffusion length. This advantage is also significantly enhanced when the diffusion length is much smaller than the absorption length. The radial p–n junctions studied here consist of micron-scale to nano-scale diameter holes etched into a copper contaminated silicon wafer. Radial p–n junctions contaminated with copper impurities show roughly a twofold increase in efficiency than similarly contaminated planar p–n junction solar cells; however the enhancement is a strong function of the radial junction pitch, with maximum enhancement occurring for a pitch that is twice the carrier diffusion length.

1. Introduction

Solar energy represents one of the most important sustainable and renewable energy sources. The most common material used in solar cells is silicon. Silicon accounts for more than 98% of the solar cell market (when amorphous cells are included) [1]. This is mainly because silicon is earth abundant, highly efficient, and air stable. Crystalline silicon solar cells have achieved efficiencies approaching 25% in the laboratory and 20% commercially [2]. Currently, however, the US receives less than 1% of its electrical power from solar cells [1]. The reason is that crystalline silicon solar cell manufacturing and installation remains prohibitively expensive. One of the reasons for the high cost of crystalline silicon is the expense required to purify metallurgical-grade silicon (99% pure) to solar-grade silicon (99.99999% pure) [3]. If solar cells are to become commercially competitive, the ultimate goal is to achieve a cost to power ratio under one dollar per watt [4].

One strategy that would help achieve this goal is to manufacture radial p–n junction solar cells from metallurgical-grade silicon (MGS) or upgraded-MGS. MGS is the raw, unpurified silicon reduced from quartz in an arc-furnace. Its cost basis is roughly $1–5 per kg, making it almost 100 times less expensive than solar-grade silicon [3]. Metallurgical-grade silicon contains many metal impurities such as Fe, Al, Cu, Ti, etc. [3]. Some impurities are not uniformly distributed but tend to form metal-silicide particles, especially transition metal impurities [5]. Many of the impurities in metallurgical-grade silicon are also deep level traps [6]. Consequently, metallurgical-grade silicon solar cells suffer high recombination rates, leading to dramatically reduced efficiency. Past studies have shown the detrimental effects of individual metal impurities on the efficiency of silicon solar cells [7]. All the impurities studied degrade the efficiency significantly by decreasing the minority-carrier diffusion length. Typical diffusion length values are smaller than 10 μm for impurity concentrations above 10^{16} cm^{-3} [8].

Recent theoretical and experimental studies indicate that changing a planar p–n junction geometry to a radial p–n junction geometry may allow for high efficiencies for solar cells materials with short diffusion lengths [9–13]. In a typical planar p–n junction solar cell, charge separation and collection is in the same direction as the incident light. The majority of photo-generated electron–hole pairs outside of the p–n junction are collected only if they are within a diffusion length away from the junction. This is because the diffusion length sets the average distance an electron–hole pair may travel before recombination. Recombination results in a loss of the electron–hole pair and thus no current production. Therefore, large diffusion lengths necessitate the use of high-purity silicon materials with low trap densities. Minority-carrier diffusion lengths of several hundreds of microns in solar-grade silicon are typical [14].

The key feature of radial p–n junctions is that carrier collection is to a significant extent orthogonal to light collection. This means that shorter carrier collection distances (<10 μm) are possible. Therefore, as light is absorbed throughout the entire cell thickness, the carriers have a much shorter collection pathway to traverse before recombination can occur [11]. Radial p–n junctions can be fabricated using any rod-like structure. For optimal performance, the radius of the 'rods' should not exceed the minority-carrier diffusion

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length, $L = \sqrt{D\tau}$, where τ is the recombination lifetime and D is the diffusion constant. Therefore, for small diffusion lengths micro- to nanostructures are desirable. The recombination lifetime is inversely proportional to the trap density. In high-purity silicon wafers with a trap density $< 10^{14}\,cm^{-3}$, τ is 1 μs or longer, which corresponds to a diffusion length from hundreds of micrometers to several millimeters long. However, in silicon with trap densities on the order of $10^{18}\,cm^{-3}$ diffusion lengths range from 100 nm to 10 μm, so that nanostructures are required to improve material performance.

In this work, we have used copper contaminated silicon to investigate the potential advantages of radial p–n junctions over their planar counterparts. Copper is chosen because it easily diffuses through silicon and is a constituent in MGS [15,16]. Copper can diffuse through a 500 μm thick silicon wafer in 14 h at room temperature [15]. Copper is also known to degrade the efficiency of silicon solar cells at concentrations above $10^{16}\,cm^{-3}$ [8,17,18].

2. Experimentals

Boron doped (p-type) silicon wafers with resistivity of 5–10 Ω cm were cleaned in a piranha solution for 10 min. The back surface of the wafer was first coated with 1 μm of aluminum by sputter deposition. Aluminum highly dopes the back surface p-type through subsequent high temperature diffusion at 850 °C in N_2 for 90 min. Aluminum doping serves two purposes: (1) the highly doped p-type silicon allows for excellent ohmic contact to the rear metallic contact, and (2) aluminum is a known getter of impurities within silicon thereby increasing minority-carrier diffusion lengths [16]. Sheet resistances are subsequently measured with a four-point probe after Al diffusion and fall within a range of 20–30 Ω/□. Ohmic contact to the p-doped layer was confirmed by observing a linear current–voltage relationship between two independent back contacts. A thin layer (≈75 nm) of copper was subsequently sputtered onto the top polished surface. Afterwards, the copper diffused through the silicon wafer through a high-temperature anneal (950 °C) in N_2 for 5 h. The Al was deposited and annealed first at high temperature before copper deposition and annealing. This was done to minimize out-diffusion of copper to the surface and thereby maintain a more homogenous distribution of copper impurities within the bulk silicon, since copper diffusion is fast at elevated temperatures [15]. After annealing, the wafer was rapidly cooled [17] and then placed into a solution of copper etchant consisting of $FeCl_3$ and water (Transene CE-100). This step removed any residual copper on the surface and the polished surface of the wafer was recovered.

Secondary Ion Mass Spectroscopy (SIMS) studies confirmed that the silicon wafer was contaminated with copper impurities (Figure 1). The copper concentration is highest at the surface and steadily decays to levels throughout the bulk consistent with the solid solubility of copper in silicon. The copper concentration is determined by monitoring complex positively charged secondary ions using a cesium ion gun. Specifically, these were ions of atomic mass units 161 and 196, which correspond to $CsSi^+$ and $CsCu^+$, respectively. The etch rate of the silicon surface was 1.7 nm/s and the concentration of copper atoms was found by multiplying the normalized copper mass counts by the sensitivity factor of the SIMS instrument. The copper signal detected by SIMS shows that the copper distribution is highest near the surface at 1×10^{20} Cu atoms/cm^3 and plateaus above 1×10^{17} Cu atoms/cm^3 within the bulk (Figure 1). The copper diffusion extends at least 6 μ into the silicon, which is similar to the depth of the radial trenches that are etched in subsequent steps (see below). Copper is known to form copper silicide precipitates at the temperature (950 °C) used during the diffusion process [19]. The inhomogeneous distribution of copper as shown by SIMS is consistent with previous observations of copper silicide formation [15]. Copper silicide is known to significantly decrease minority-carrier diffusion lengths to values less than 20 μm [8,17]. At this stage, the copper contaminated wafer is ready for radial p–n junction fabrication.

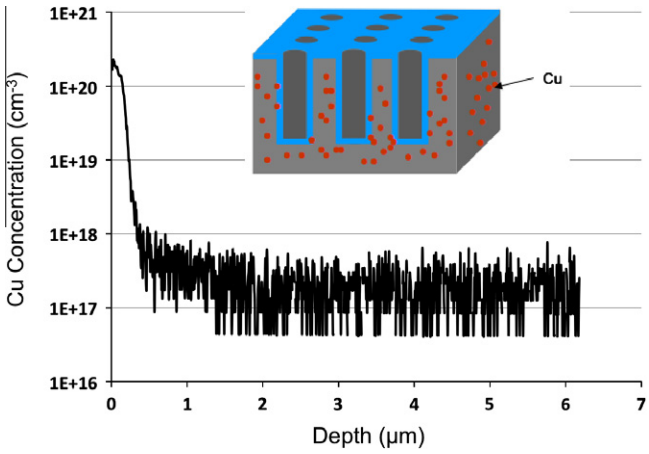

Figure 1. Secondary Ion Mass Spectroscopy (SIMS) data collected as a function of depth on a silicon sample contaminated with copper at 950 °C. The data was collected by monitoring positively charged copper ion species as they were removed by a cesium ion gun. Normalized atomic masses were multiplied by the sensitivity factor of the SIMS instrument. The copper concentration is highest near the surface 1×10^{20} Cu atoms/cm^3 but eventually plateaus to a constant level $\sim 1 \times 10^{17}$ Cu atoms/cm^3 throughout the bulk that is near the solid solubility of copper.

The radial p–n junctions are formed via a top-down approach using either optical or nanoimprint (NIL) lithography and standard CMOS compatible processes. Photolithography and NIL was used to define the hole diameter and pitch of the hole array. I-line photoresist was used and an exposure time of 2 s followed by a rinse in developer for 30 s. The pattern was transferred into the copper contaminated silicon wafer via a deep reactive ion etch (DRIE) (Figure 2). An etch mask consisting of 50 nm of silicon dioxide was used during the DRIE process. The etch mask was grown by thermal oxidation of the copper contaminated silicon wafer. The DRIE process etched the silicon 6–10 μ deep (Figure 2c).

The array of holes occupied an area of 5 mm by 5 mm. The diameter of all holes fabricated via photolithography was 2 μm and the pitch was either 4 or 10 μm for different devices (Figure 2b and c). By contrast, the diameter of all holes fabricated via NIL was 370 nm with a pitch of 500 nm. The holes were then filled with a phosphorus-containing spin-on glass by spin coating at 4000 revolutions/min and baking on a hot plate at 250 °C for 5 min. The wafers were then annealed at 930 °C for 7 min to drive in the phosphorus. This resulted in a ≈250 nm thick n^+ layer on the sidewalls of the holes and the top surface of the wafer. Afterwards, the spin-on glass was removed by a 30 s HF dip. The sheet resistance of the n-type layer was measured with a four-point probe and values ranging from 60 to 70 Ω/□ were obtained. Finally, top finger contacts using Au/Ti (100/10 nm) were applied to the n+ layer and the bottom surface of the wafer was metalized with 100 nm of Al by e-beam deposition. The finger contacts are 30 μm in width and are separated by 800 μm.

Individual devices were secured onto a gold-coated chip carrier with silver paste. Sputtered silver finger contacts that were 1 μm thick, 30 μm wide, and spaced 800 μm apart, were used for the top contacts [20]. Wire bonding onto the top finger contacts completed the circuit. The devices were then loaded onto a stage that has been calibrated to receive 100 mW/cm^2 photon flux (1 sun) through an atmospheric mass (AM) 1.5 filter. *I–V* measurements

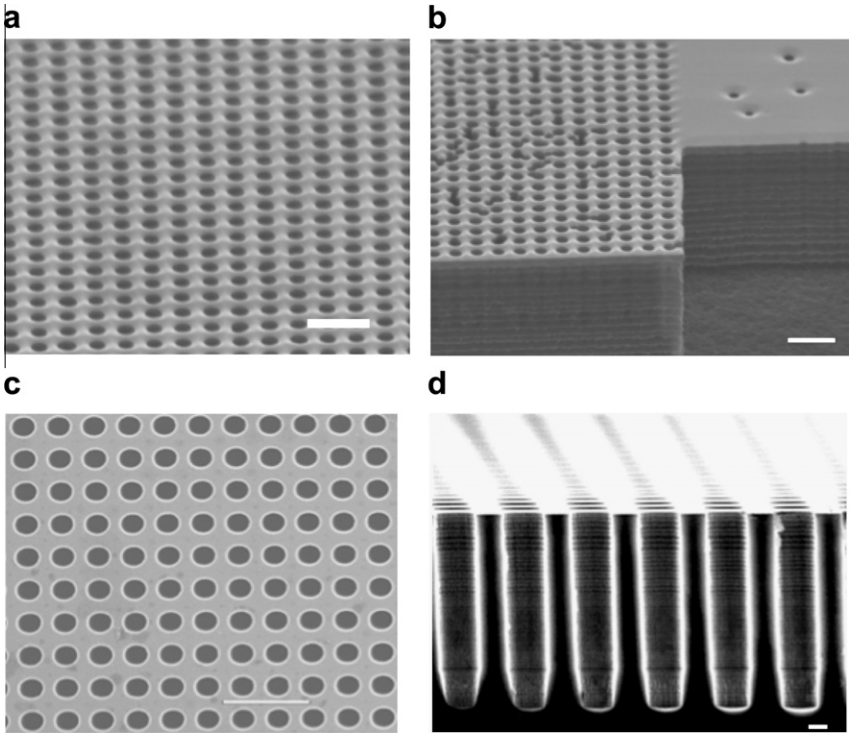

Figure 2. (a) A SEM image of an array of holes generated by nanoimprint lithography (NIL) in a copper contaminated p-type wafer. The hole diameter is 370 nm and the pitch is 500 nm. (scale bar is 1 μm). (b) Cross sectional SEM of a NIL device (scale bar is 1 μm). (c and d) SEM image of an array of holes generated by photolithography in a copper contaminated p-type wafer. The hole diameter is 2 μm and the pitch is 4 μm (scale bar is 10 μm). (d) A cross sectional SEM of a representative device. The trenches are 8 μm deep and are etched by DRIE using the Bosch process, which consists of an alternating gas flow of SF_6 etching and C_4F_8 passivation (scale bar is 1 μm). The radial p–n junction is formed by diffusing phosphorus into the sidewalls of the holes at elevated temperatures using a spin-on dopant, which is then removed by a HF etch.

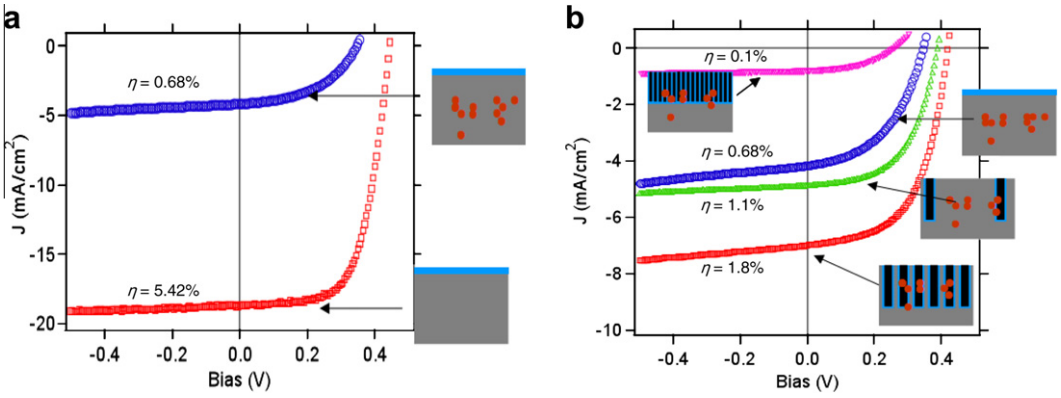

Figure 3. (a) *I–V* data at 100 mW/cm^2 (1 sun and AM 1.5) for a 'clean' planar (red trace) and 'dirty' planar (blue trace) p–n junction solar cell device. The efficiency is 8% and 0.68%, respectively. The efficiency decreases due to the presence of copper impurities. (b) *I–V* data at 1 sun and AM 1.5 for planar and photolithographically defined radial devices which were copper contaminated. The radial device with 4 μm pitch (red trace) has the largest short-circuit current and thus the largest efficiency (1.8%). The radial device defined by nanoimprint lithography with the smallest pitch (500 nm) (purple trace) has the smallest efficiency at 0.1%. The 'dirty' radial device with 10 μm pitch has an efficiency of 1.1%.

were conducted on two types of samples: electronic grade ('clean') planar and radial p–n junction devices and copper contaminated ('dirty') planar and radial p–n junctions (Figure 3). The planar devices were used as controls to show the difference if any from the radial devices and were always fabricated from the identical wafer used for the radial p–n junctions.

Electron Beam Induced Current (EBIC) measurements were carried out to directly estimate the electron diffusion lengths for the clean and dirty Si used in our devices (Figure 4). The electron beam in a scanning electron microscope is rastered along the surface of the semiconductor and generates electron–hole pairs which are then separated and collected by a Schottky junction often-formed by a metallic probe tip. The short-circuit current is measured as a function of beam position by an ammeter. This results in a map of the short-circuit current and can indicate the presence of impurities. A tungsten probe tip mounted on a nanomanipulator inside the SEM was used to make a Schottky contact with the top surface of the p-Si wafer [21]. A large area ohmic contact was fabricated by

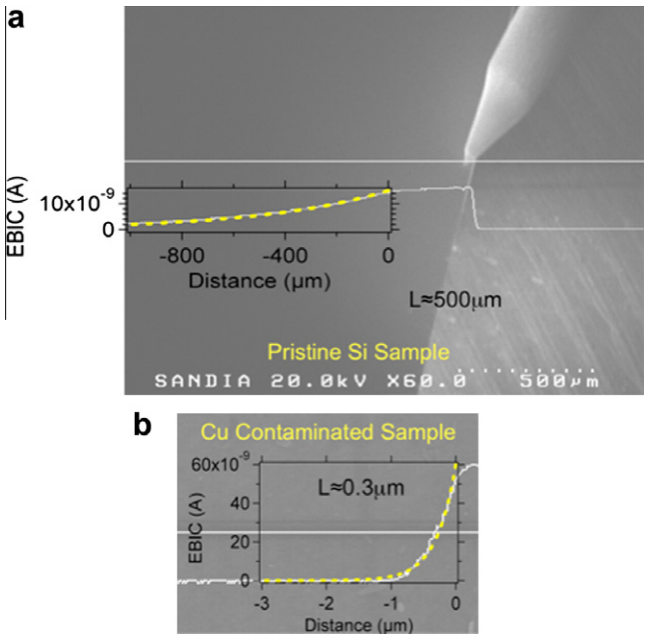

Figure 4. Electron Beam Induced Current (EBIC) measurements were performed to ascertain the electron diffusion length. (a) The short-circuit current as a function of distance from the Schottky barrier formed by a tungsten probe and silicon surface is shown. A single exponential fit to the current decay yields a diffusion length of ≈500 μm for the clean silicon sample. (b) A single exponential fit to the current decay for a sample contaminated with copper at 750 °C yields a diffusion length of ≈ 300 nm.

applying In metal with a soldering iron onto the backside pre-scratched using a diamond scribe (two such contacts were made to ensure ohmic character). EBIC current was recorded using a variable gain amplifier interfaced with the SEM video input. All measurements were carried at an accelerating voltage of 20 kV, corresponding to electron penetration depth of approximately 3.5 μm [22].

3. Results and discussion

For clean devices, the largest efficiency (5.42%) is observed for the planar geometry (Figure 3a), while the 'dirty' planar device has an efficiency of 0.68%. By contrast, for the dirty radial devices, the highest efficiency is observed for the device with the 4 μm pitch (≈1.8%) (Figure 3b) and arises due to a larger short-circuit current, indicating that the radial p–n junction architecture is effectively collecting minority carriers. The device with 10 μm pitch has an efficiency of 1.1%. Interestingly, the NIL devices have the smallest efficiency at 0.1%. This unexpected result is due to depletion effects at the very small pitch, as explained by modeling results below. Reflectance measurements were performed to rule out any significant contributions from an increase in absorption for the array of holes. Reflectance data show a negligible contribution (reflectance is ≈10% smaller) for the radial geometry devices.

SEM images of the 'clean' and 'dirty' Si specimens contacted by the tungsten probe along with the EBIC signal traces are shown in Figure 4. Superimposed over the EBIC traces are curve fits to an exponential decay function [23].

$$I = I_0 \exp(-x/L_D)$$

where I is the EBIC current, I_0 is a constant, x is the distance from the space charge region, and L is carrier diffusion length. This formula is readily derived from kinetic equations. Based on the EBIC data, we estimate a diffusion length of ≈500 μm for the clean Si, and ≈0.3 μm for the copper contaminated Si. This very low diffusion length is likely the result of surface segregation of Cu impurities, as evident from the SIMS data in Figure 1. The lower Cu contamination of $10^{17}/cm^3$ in the bulk of the wafer would imply a carrier diffusion length of several tens of micrometers [16]. However, the damage associated with the DRE process is likely to getter Cu impurities from the bulk resulting in higher Cu concentration in the vicinity of the pn-junction, where it would have the most impact on device performance. To determine whether the EBIC measured diffusion length was consistent with the photovoltaic measurements, we fit I–V curves collected for the 10 and 4 μm pitch devices to an analytical model based on the work of Kayes et al. [11]. This model works well as long as the radial junctions can be treated as isolated devices and yields a minority-carrier diffusion length of ≈0.1 μm, consistent with the EBIC measurement.

These diffusion lengths measurements illustrate the advantage of utilizing a radial p–n junction architecture. Minority carriers in the copper contaminated radial junction devices are collected at a higher rate than their planar counterparts, which is evident from the increased short-circuit current. This is because the carrier collection distance, on average, is much shorter (by two orders of magnitude) than the planar junction devices. Therefore, the radial p–n junction architecture maintains an appreciable short-circuit current in the presence of copper impurities. No decrease in the open circuit voltage, (which is expected to decrease due to a larger junction area), is observed for the cells with 2 μm diameter holes. This indicates that the short-circuit current counteracts the deleterious effects of large junction area. For the device with 0.13 μm diameter holes the radial junction contribution to the total collected photocurrent is nearly zero (see model below), leading to the observed lower open circuit voltage.

We next present modeling results in order to understand the dependence of the radial p–n junction array performance on pitch. Previous modeling of the radial p–n geometry has considered a single junction [4], and is therefore directly applicable to nanorod arrays in the limit of large pitch (larger than twice the diffusion length). For pitch smaller than this, the charge collection and electrical properties of junctions are not independent. To capture the geometrical dependence of system behavior in this regime, we use a numerical approach. We solve the standard drift–diffusion and Poisson equations in two-dimensions using the Scharfetter–Gummel finite-difference scheme [23]. The top and bottom boundaries represent charge collecting contacts, and we apply periodic boundary conditions for the right/left edges (see Figure 5a inset for system geometry). We assume a spatially uniform charge generation rate $G = 10^{-10}(N_v D/x_0^2)$, where D and x_0 are the diffusion constant and Debye length, respectively, and N_v is the valence band edge density (assumed equal to the conduction band edge density). We use Read–Shockley–Hall recombination $R = (np - n_i^2)[\tau_n(p+n_i) + \tau_p(n+n_i)]^{-1}$, with $n_i^2 = n_0 p_0$, $\tau_n(\tau_p)$, the electron (hole) lifetime, and $n_0(p_0)$ the electron (hole) equilibrium density; we take trap state energies to be mid-gap and use $\tau_n = \tau_p = 10^5(x_0^2/D)$. We take $k_BT = 1/40$ eV, $E_{gap} = 1$ eV, and doping levels $N_D = 0.1N_v$, $N_A = 0.001N_v$. The geometry of doping is shown in the inset for Figure 5a; we choose $h = 5500x_0$, total unit cell height $7500x_0$, the width of acceptor region is varied, and the width of donor is set to $100x_0$. We assume the contacts are minority blocking, so that the recombination velocity S of majority and minority carrier are: $S_{maj} = 10^7(D/x_0), S_{min} = 10^{-3}(D/x_0)$.

The behavior of the junction array as a function of pitch can be understood in terms of the length scales of a single, 1-dimensional p–n junction in the regime of $N_D \gg N_A$. The important length scales are the diffusion length $L_D = \sqrt{\tau D}$, the depletion width $w_p = \sqrt{\frac{2\varepsilon\Delta\phi}{N_A}}$, and the n–p crossover point (the distance x_{pn} away from the interface where $n(x_{np}) = p(x_{np})$): $x_{np} = w_p(1 - \frac{1}{\sqrt{2}})$. We find that the biggest effect of decreasing the pitch is on the short-circuit current.

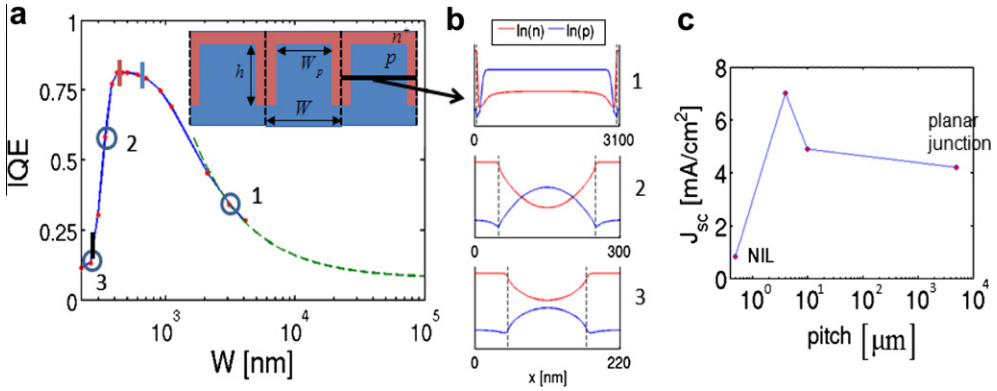

Figure 5. (a) Model results for internal quantum efficiency versus inter-rod spacing W_p. The dashed green line is the asymptotic form of IQE, as described in the text. Inset shows device geometry, $h = 5500$, $W = W_p + 100$. Blue (red) line on IQE curve shows W_p value where diffusion length (depletion width) of two interfaces overlap, black line shows where rods no longer form p–n junction. (b) Cross sections through a unit cell of log(carrier density) for three values of W_p: (1) shows widely separated rods, (2) shows regime of depletion width overlap, (3) shows regime with no p–n junction. (c) The experimental short-circuit current versus pitch shows qualitative features consistent with the modeling result.

We therefore focus on the short-circuit current, and express it in the equivalent form of the internal quantum efficiency (IQE).

Figure 5a shows the IQE as a function of pitch, illustrating four distinct regimes. Regime 1: for large inter-rod spacing, simple geometrical considerations imply that the current collected in a unit cell of width W is proportional to perimeter of the junction. For a junction height h, this is simply $W + 2h$, implying a pitch-dependence of the short-circuit current density of $1 + \frac{2h}{W}$ (dashed green line in Figure 5a). Regime 2: as the pitch is reduced below $2L_D$, the IQE begins to saturate. This is because the collection area of one interface overlaps a region where charge was already being collected by the other interface; the extra interface therefore adds no further benefit, and we reach a state of 'diminishing returns'. Regime 3: when the pitch is sufficiently small so that depletion regions of adjacent junctions overlap, we observe a sharp drop in IQE. This is because overlapping depletion regions preclude carrier densities from relaxing to the asymptotic values of single junctions: the majority density maximum value is reduced, and the minority density minimum value is increased. The increase in the minority carrier density increases recombination, resulting in less collected charge and a reduced IQE. Regime 4: when the pitch is smaller than the n–p crossover distance x_{np}, there is no longer space to accommodate a crossover from n-type to p-type, and the vertical sections of the rods no longer operate as p–n junctions. At this point, only the horizontal junction contributes to charge collections, and the structure effectively operates as a planar junction.

Some features of the geometrical dependence we describe above are unique to 2-dimensions (such as the $1 + \frac{2h}{W}$ dependence of IQE on W). These will be modified in an obvious way for the full 3-dimensional system (in this case the IQE for rods of radius R should scale as $1 + \frac{2\pi Rh}{W^2}$). Moreover, the specific shape of the IQE versus pitch should change as well, but it is clear that qualitatively similar transitions in performance should arise as adjacent junctions approach each other and important regions surrounding the junctions (e.g. depletion regions) overlap.

4. Conclusion

We have fabricated and characterized copper contaminated radial p–n junction solar cells. Our experiments have shown that radial p–n junction geometry can result in improved efficiencies compared to the planar p–n junction devices for silicon samples contaminated with copper. Based on our experimental results and a 2-dimensional model, we have shown that performance of radial p–n junction array solar cells is a strong function of nearest neighbor distance, reaching a maximum at approximately twice the carrier diffusion length, and rapidly degrading as the distance becomes shorter than twice the depletion width.

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Akram Boukai obtained dual undergraduate degrees in electrical engineering and chemistry from UCLA. At UCLA he was awarded the Dolores Cannon Southam Award for excellence in undergraduate research. Akram then obtained his Ph.D. from Caltech in chemistry and studied the thermoelectric properties of bismuth and silicon nanowires. He was awarded a Gold Medal at the spring 2008 MRS conference in San Francisco for his work on silicon thermoelectrics. Afterwards, Akram was a post-doctoral scholar at UC Berkeley in the lab of Professor Peidong Yang. Currently, Akram is an Assistant Professor in the Materials Science and Engineering Department at the University of Michigan.

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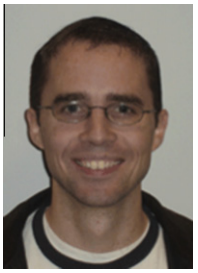

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