Light Induced Charge Transport within a Single Asymmetric Nanowire

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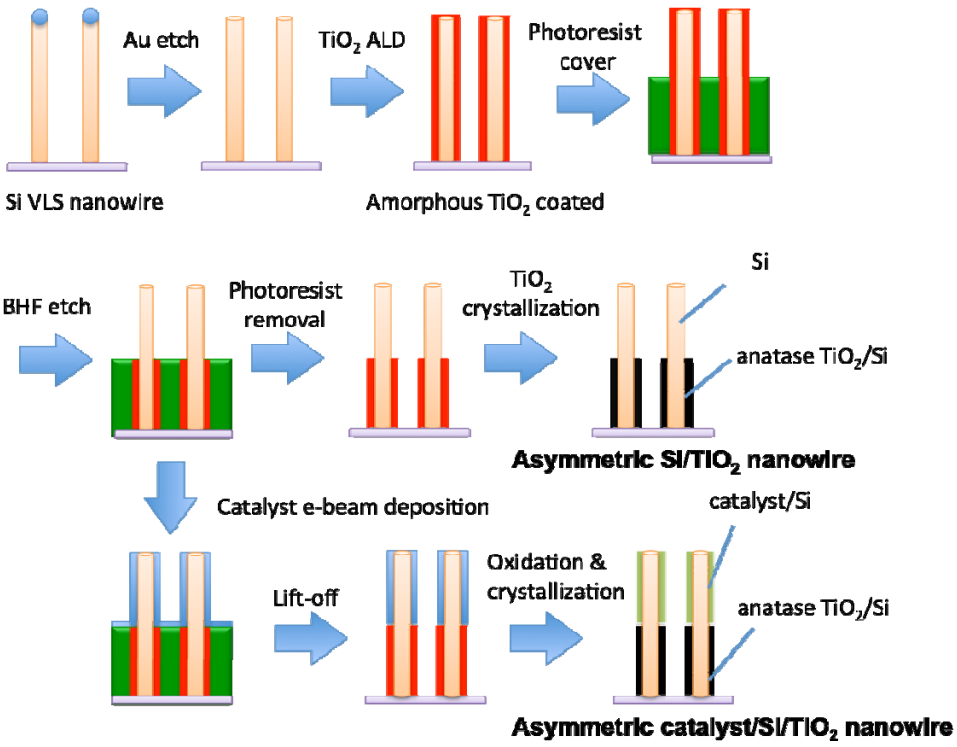
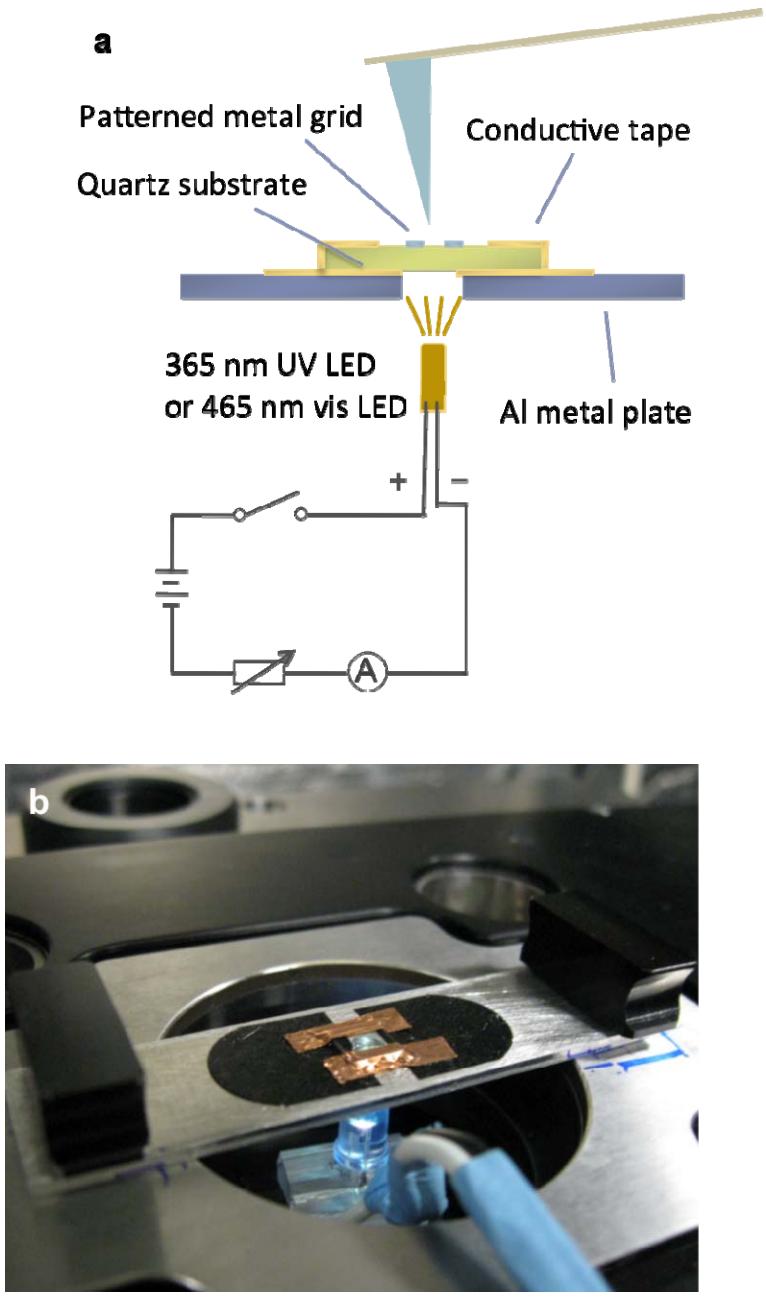
Methods

Asymmetric Si/TiO_2 nanowire fabrication. Detailed synthesis scheme of the asymmetric nanowires is shown in Figure S1. The asymmetric Si/TiO_2 nanowire started from a VLS grown Si nanowire on a p-Si(111) wafer (10-20 Ωcm) pre-coated with 80 nm Au nanoparticle colloid solution (Ted Pella Inc.) by the method described previously (ref. 22 in paper). The Si nanowires were grown at 850°C, with Ar (10% H_2) bubbled through the $SiCl_4$ precursor at 0°C. The nanowire array was then subjected to an HF vapor etch, KI/I_2 Au etchant to remove the Au seed particles, and the 30 nm amorphous TiO_2 conformal coating at 80°C in a home-built ALD system using $TiCl_4$ and H_2O as precursors. Ethyl acetate diluted G-line photoresist (Microchem Corp.) was drop-cast onto the substrate to cover the bottom half of the Si/TiO_2 core-shell structure. After baking at 100°C, the sample was immersed in 1:5 buffered HF (BHF) solution to etch the amorphous TiO_2 layer not protected by the photoresist. After removal of the photoresist by O_2 plasma, post-annealing was applied to crystallize the TiO_2 to anatase at 600°C for 1h.

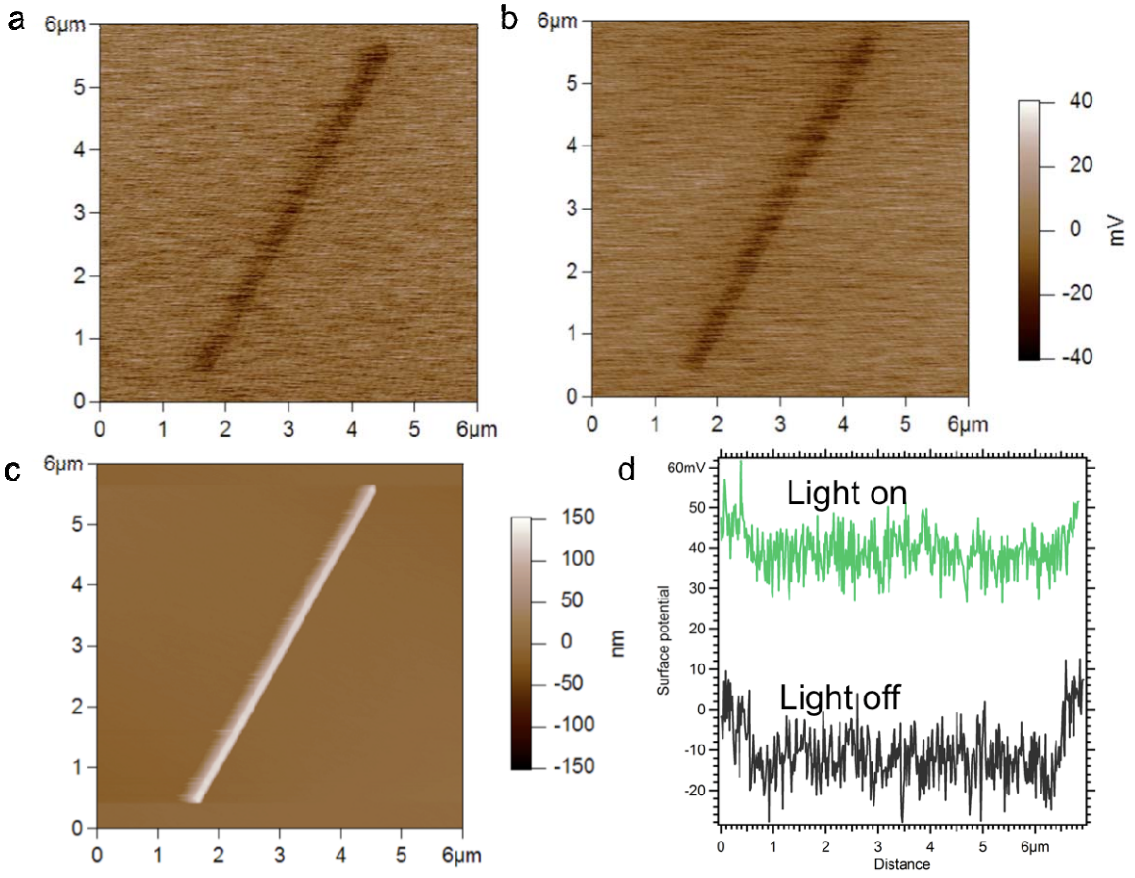
KPFM measurement KPFM measurements were performed in an Asylum MFP-3D^{TM} stand-alone AFM equipped with AEK 2002 acoustic isolation hood. The experimental setup is shown in Fig. S2. In detail, an asymmetric nanowire was transferred to a fused silica substrate patterned with Au lines to minimize the effect of static charge. The quartz substrate was placed on top of an aluminum sample stage. 2.5 mW, a 365 nm UV LED (T-1 ¾ package, NICHIA Inc.) or 20mW 465 nm LED (T-1 ¾ package, Thorlabs Inc.) was positioned ~0.5 mm underneath the quartz substrate to realize diffusive illumination. KPFM measurements were carried out in AC mode using the technique reported before [citation?], with 50 nm lift distance. A typical 512-by-512 pixel scan was run at 0.5 Hz over 10×10 μm^2 with a Nanoworld PointProbe^{TM} EFM cantilever under the controlled humidity at 60~70% r.h. Changing the light intensity was achieved by controlling the current through the LED with an external circuit, and the light intensity was measured based on the ratio of overall optical power passing through the hole of sample stage (measured by a calibrated photodiode from Newport Inc.) to the area of the hole.



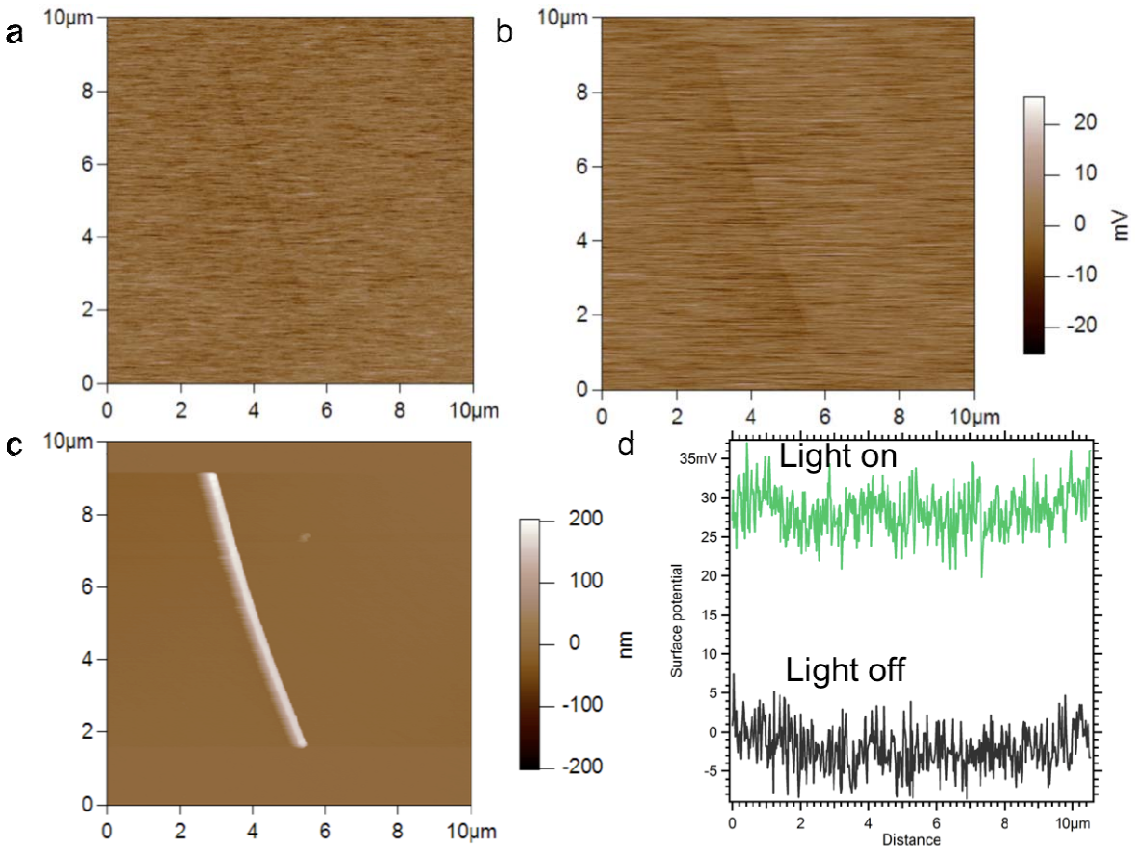
Supplementary Figure S1. A generalized scheme for fabrication of the asymmetric nanowires. The Si VLS nanowire in the first step was synthesized using either 80 nm Au nanoparticles or Au thin film deposited on the soft-lithographically patterned substrate.



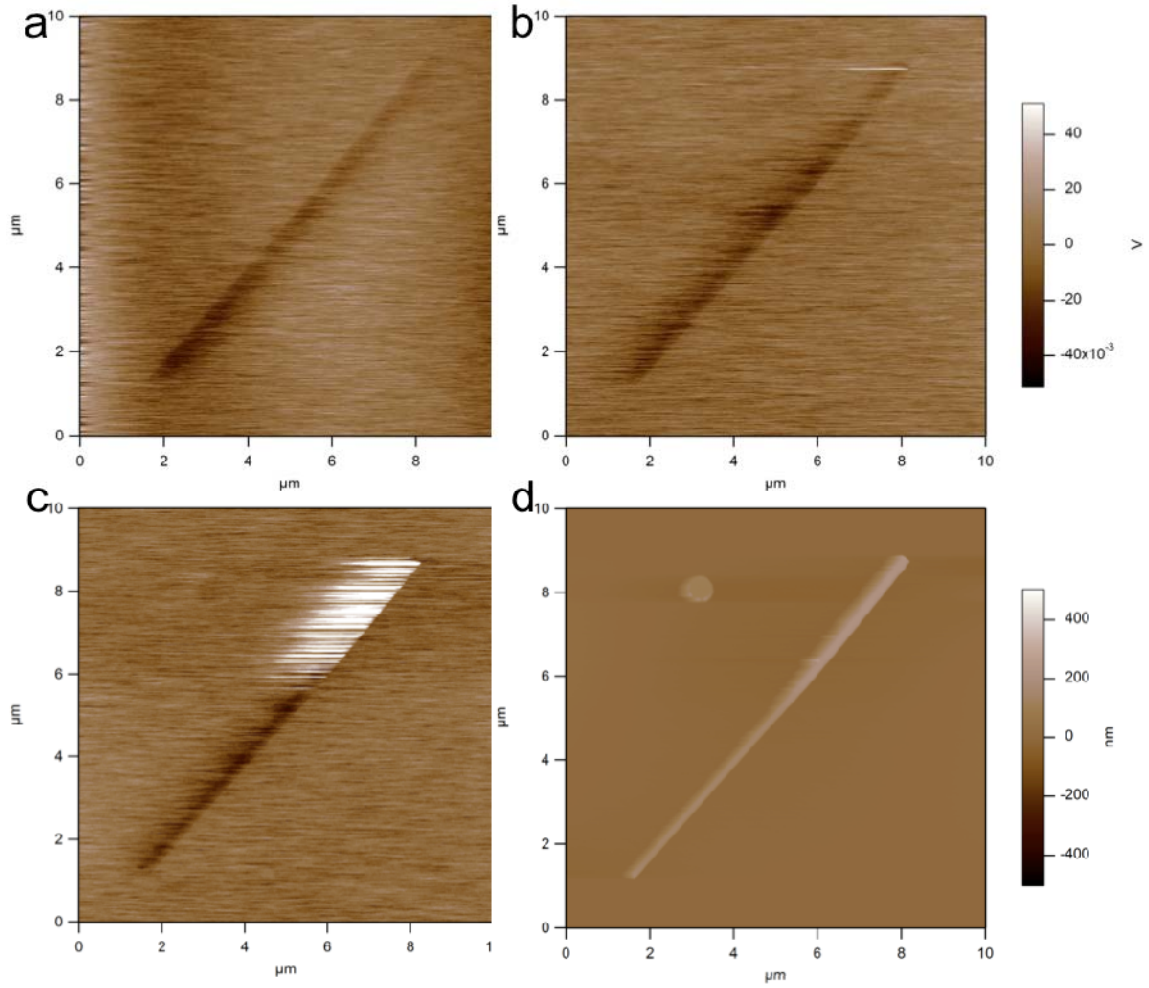
Supplementary Figure S2. Schematic illustration (**a**) and photograph (**b**) of the KPFM setup with backside LED illumination.



Supplementary Figure S3, Surface potential profile of a Si nanowire in the dark (**a**) and under 365 nm UV illumination (4.5 mW/cm^2) (**b**). **c**, topographical image of the Si nanowire. **d**, comparison of the surface potential along the nanowire in the dark (black) and under illumination (green).



Supplementary Figure S4, Surface potential profile of a Si/TiO_2 core-shell nanowire in the dark (**a**) and under 365 nm UV illumination (4.5 mW/cm^2) (**b**). **c**, topographical image of the Si/TiO_2 core-shell nanowire. **d**, comparison of the surface potential along the nanowire in the dark (black) and under illumination (green).



Supplementary Figure S5, Surface potential profile of an asymmetric Si/TiO_2 nanowire in the dark (**a**), under 465 nm visible illumination (4.5 mW/cm^2) (**b**), and under 365nm UV illumination (4.5 mW/cm^2) (**c**). **d**, topographical image of the asymmetric Si/TiO_2 core-shell nanowire.