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Simultaneous Thermoelectric Property Measurement and Incoherent Phonon Transport in Holey Silicon

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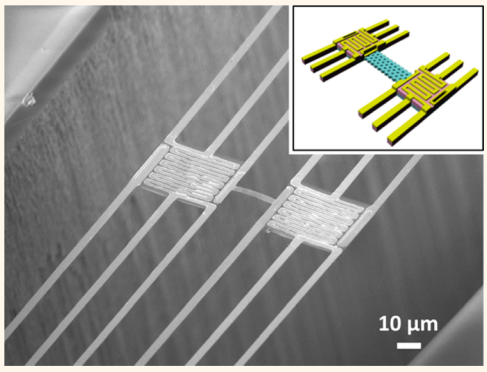
Supporting Information

ABSTRACT: **Block copolymer patterned holey silicon (HS) was successfully integrated into a microdevice for simultaneous measurements of Seebeck coefficient, electrical conductivity, and thermal conductivity of the same HS microribbon. These fully integrated HS microdevices provided excellent platforms for the systematic investigation of thermoelectric transport properties tailored by the dimensions of the periodic hole array, that is, neck and pitch size, and the doping concentrations. Specifically, thermoelectric transport properties of HS with a neck size in the range of 16−34 nm and a fixed pitch size of 60 nm were characterized, and a clear neck size dependency was shown in the doping range of 3.1 × 10^{18} to 6.5 × 10^{19} cm^{-3}. At 300 K, thermal conductivity as low as 1.8 ± 0.2 W/mK was found in HS with a neck size of 16 nm, while optimized zT values were shown in HS with a neck size of 24 nm. The controllable effects of holey array dimensions and doping concentrations on HS thermoelectric performance could aid in improving the understanding of the phonon scattering process in a holey structure and also in facilitating the development of silicon-based thermoelectric devices.**



KEYWORDS: *thermoelectrics, silicon nanostructure, holey silicon, phonon transport, thermal conductivity*

Recent exploitation of nanostructured materials has stimulated a renewed interest in thermoelectric power generation from solar, automobile, and industrial heat sources.[1−3] The heat-to-electricity conversion efficiency of thermoelectric modules is associated with the material-dependent figure of merit, $zT = \sigma S^2 T/\kappa$, where σ, S, κ, and T are electrical conductivity, the Seebeck coefficient, thermal conductivity, and absolute temperature, respectively. The Seebeck coefficient is based on an open-circuit voltage induced in a semiconductor under a thermal gradient, and it scales inversely with the carrier concentration. The thermal conductivity contains contributions from both phonons (lattice vibrations) and electrons. To produce useful power from heat sources, a low electrical resistivity in a degenerate carrier doping range (*i.e.*, 10^{19}−10^{20} cm^{-3}) is required for maximizing the thermoelectric power factor (σS^2). When attenuating phonon transport is done without adversely affecting electron transport, zT is no longer constrained by the interplay of the three material properties.[4−6] As a result, power generation efficiency of thermoelectric modules would be greatly improved for practical application.

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Silicon has been considered for thermoelectric application, as it is abundant and its processing techniques are well-developed. Yet, the overall thermoelectric performance of silicon is very poor (zT < 0.01 at 300 K), due to the high thermal conductivity (~150 W/mK at 300 K).[7,8] It was demonstrated that nanostructured silicon could effectively damp phonon transport without causing severe electron scattering[9,10] when it has a limiting dimension between mean free paths (MFP) of phonons (~300 nm) and electrons (<10 nm) of degenerately doped silicon.[11] Hochbaum *et al.* showed that rough silicon nanowires have a largely suppressed thermal conductivity, a minor deterioration in thermoelectric power factor, and an enhanced zT ~ 0.6 at 300 K.[9] Further, Lim *et al.* experimentally showed that a high-frequency surface roughness is essential to suppress the thermal conductivity of silicon nanowires.[12] While these nanowire systems exhibit excellent properties, the challenge of controlling the roughness of silicon nanowires at a large scale has promoted the development of the alternative structure, holey silicon (HS).[10]

HS is single-crystalline silicon containing an array of periodic holes that are several tens of nanometers in diameter. For HS, a nontrivial zT ~ 0.4 at room temperature has also been reported by Tang *et al.*, based on a large reduction in the thermal conductivity.[10] With a neck/pitch size of adjacent holes (illustrated in Figure 1) = 23/55 nm and a membrane thickness of 100 nm, the thermal conductivity of the HS membrane is reduced to ~1.73 W/mK. Yet, the degradation in thermoelectric power factor remains tolerable. The significantly reduced thermal conductivity in HS was attributed to a "necking effect", where phonons with MFPs longer than the hole spacing can be "trapped" behind hole, as illustrated by the Monte Carlo (MC) simulation of Hao *et al.*[13] As such, hole surfaces, scattering ballistic phonons, would be locally heated to cause a negative temperature gradient locally behind holes.

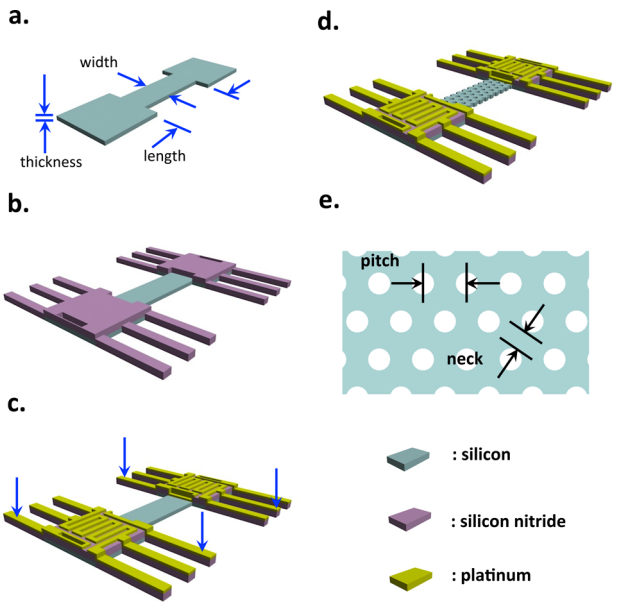

Figure 1. Schematic of the integrated microdevice. (a) Silicon ribbon consists of two end pads (30 × 40 μm) for making thermal contacts with low-stress SiN_x pads. The length, width, and thickness of the silicon ribbon are defined and used for extracting the thermal and electrical conductivity from the measurements. (b) Six legs of low-stress SiN_x for each end pad are used to suspend the silicon ribbon microdevice. The two Si/SiN_x covalently bonded pads and the Si ribbon define the thermoelectric measurement platform. (c) Control silicon ribbon (without holes) microdevice. Four-point ohmic contacts (Cr/Pt = 2/30 nm, marked by the blue arrows) to the silicon ribbon are used for electrical measurements. The rest of the legs are four-point contacts of the two PRTs. Color codes for Si, SiN_x, and Pt are applied to all figures. (d) HS ribbon microdevice. Nanometer holes are fabricated *via* the BCP lithography. (e) Schematic showing the defined pitch size and the neck width of our HS.

Remarkable thermal conductivity reduction in silicon was also observed in similar holey structures, yet with different neck/pitch sizes.[14−18] El-Kady *et al.* reported thermal conductivities of 33−80 W/mK for 250 nm thick silicon membranes with a neck/pitch size = 200−450/500−900 nm at room temperature.[16] Yu *et al.* showed a much lower thermal conductivity of 1.9 W/mK for 20 nm thick silicon nanomesh with a neck/pitch size = 18−23/34 nm.[14] Both groups ascribed the thermal conductivity reduction to a phononic crystal effect, that is, a coherent phonon interaction that has also been found in the superlattice structures.[19−21] For coherent phonon transport, the periodicity of a hole array induces the folding of the Brillouin zone and modifies the phonon dispersion relation, wherein the phonon group velocity becomes slower and phononic stop-bands can form.[17,22] Instead, incoherent phonon scattering was discussed by fitting the experimental data of these lithography-fabricated HS samples using MC simulations in reports of Jain *et al.*[23] and Ravichandran *et al.*[24] Both works further suggested that phonon wavelength = 1−10 nm, carrying the majority of heat conduction, is much shorter than dimensions of lithographically prepared holey structures such that coherent phonon transport in these HS samples may be trivial. Considering both coherent (MFP > neck size) and incoherent phonons (MFP < neck size) using the finite difference time domain method, Dechaumphai *et al.* suggested that two different processes may both contribute to the reduced thermal conductivity of HS.[25] Recently, Alaie *et al.* postulated in their model that phonon possessing a MFP above a threshold MFP can transport coherently and successfully explained their experimental result of microporous HS (a neck/pitch size = 250 nm/1.1 μm).[17]

Current disagreement on phonon transport of HS is largely due to the lack of systematic experimental data; for instance, there is no complete data set with varying the limiting dimension, that is, the neck size, below 100 nm. Also, lattice integrity of fabricated nanoholey sample often was overlooked in experimental reports and has not been confirmed by either associated electrical properties or spectroscopy.

In this report, HS samples with tailored neck size, doping level, and ribbon geometry were investigated in order to help advance the understanding of thermoelectric transport in the unique holey structure. The transport measurements were conducted using the fully integrated HS microdevices that were fabricated by combining block copolymer (BCP) lithography with conventional photolithography. Parasitic thermal contact resistances were eliminated due to the monolithic contacts, and more importantly, all three thermoelectric properties (σ, S, and κ) could be measured from the same HS sample using this microdevice. With a fixed pitch size of ~60 nm, the neck size of HS was quantitatively varied from 16 to 34 nm, and the corresponding thermoelectric properties were characterized for three different doping levels. Raman spectroscopy was used to investigate lattice integrity of these HS. Our data indicate that phonon boundary scattering plays a critical role in the thermal conductivity reduction.

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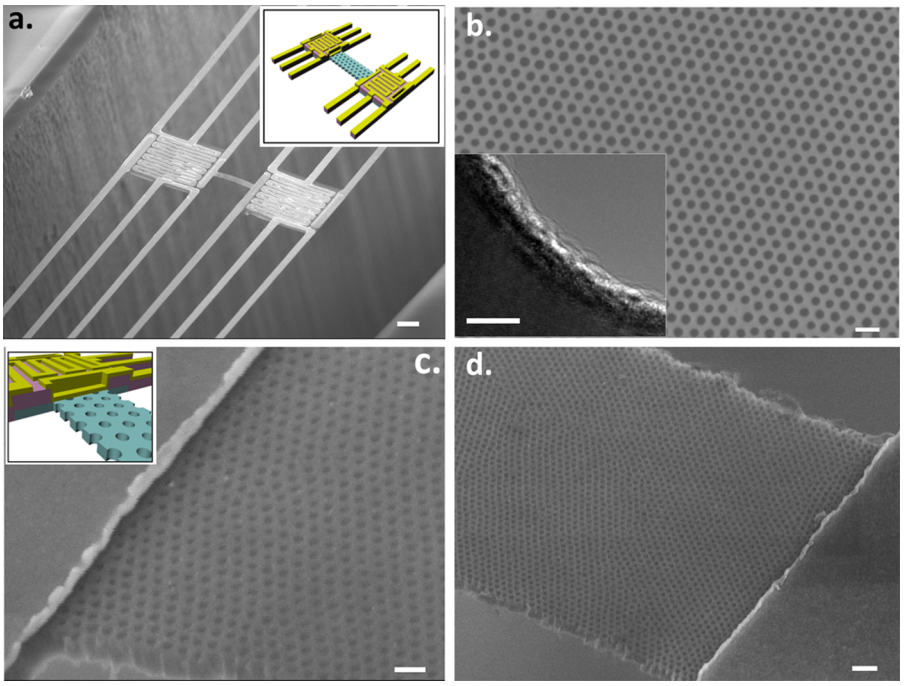

Figure 2. SEM images of the HS microdevice. (a) Low-magnification SEM image at a tilted angle of 60°. Inset is the schematic of a corresponding HS microdevice. (b) SEM image of the top view of the HS ribbon. The average neck width is 23 nm with standard deviation of 1.7 nm. Inset is the high-resolution transmission electron microscopy image, showing ~2 nm thick native oxide with smooth interfaces at the edge of hole. (d) Tilted SEM image of the HS with the monolithic Pt ohmic contact. Inset is the corresponding schematic of the interface between the HS ribbon and the Pt contact. (d) Tilted SEM image shows the long-range order of the holey structure of the HS ribbon. Scale bars are 10 μm, 100 nm (5 nm for the inset), 100 nm, and 200 nm, respectively.

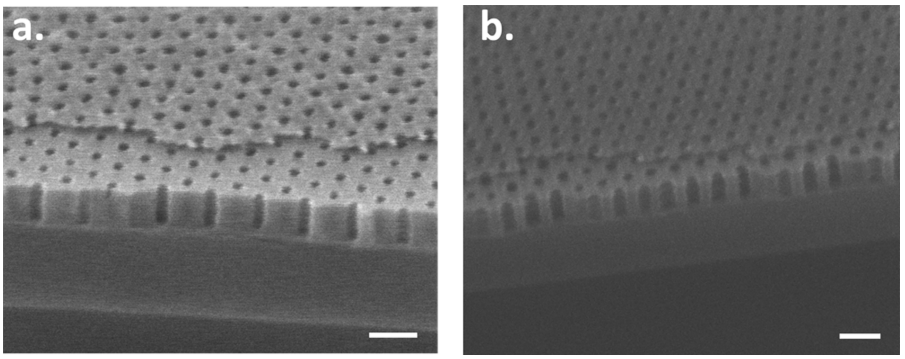

Figure 3. SEM images (tilted by 45°) of the two different HS samples with Cr holey masks after the DRIE processes. The HS porosity was calibrated by tuning Cr mask thickness and DRIE etching/passivation cycle. (a) HS porosity is ~20% (Cr 9 nm and DRIE 9 cycles). (b) HS porosity is ~34% (Cr 7 nm, DRIE 7 cycles). Scale bars are 100 nm.

RESULTS AND DISCUSSION

The fully integrated device is evolved from the previous thermal conductivity microdevice of Shi *et al.*[26] The schematics of the HS microdevice and control silicon microdevice, that is, without holes, are illustrated in Figure 1. A HS microribbon is monolithically bridged between two end pads, consisting of a heterostructure of silicon and low-stress silicon nitride (SiN_x). Each end pad is integrated with the platinum resistance thermometer (PRT), that is, Cr/Pt = 2/30 nm, *via* sputter deposition. The covalent bonding, formed by growing low-stress SiN_x on Si, effectively eliminates thermal contact resistances that have been frequently observed in either Pt/C composite bonding for nanowires (*i.e.*, deposition by focused ion beam system) or Ni bonding for microribbons (*i.e.*, deposition by e-beam evaporation).[9,10,12] In addition to the new feature of covalent bonding, four-point ohmic contacts (Cr/Pt = 2/30 nm *via* e-beam evaporation) can be directly fabricated for Seebeck coefficient and electrical conductivity measurements. As a result, we have developed a fully integrated microdevice, capable of characterizing all three thermoelectric properties of the same HS ribbon for zT assessment. Figure 2 shows the SEM images of the integrated HS microdevice. Details regarding integrating BCP lithography and microfabrication for fabricating HS microdevices are available in the Methods section and Supporting Information.

HS's thermal conductivity and Seebeck coefficient were measured simultaneously, and four-point electrical conductivity was measured in a separate cycle. The thermal conductivity measurement technique could be found in the report of Shi *et al.*[26] Briefly, at each temperature point, a DC current was applied to one PRT, creating a Joule heating on this PRT pad (hot side). A part of heat flowed through a HS ribbon and raised the temperature of the other PRT pad (cold side). The heat flux

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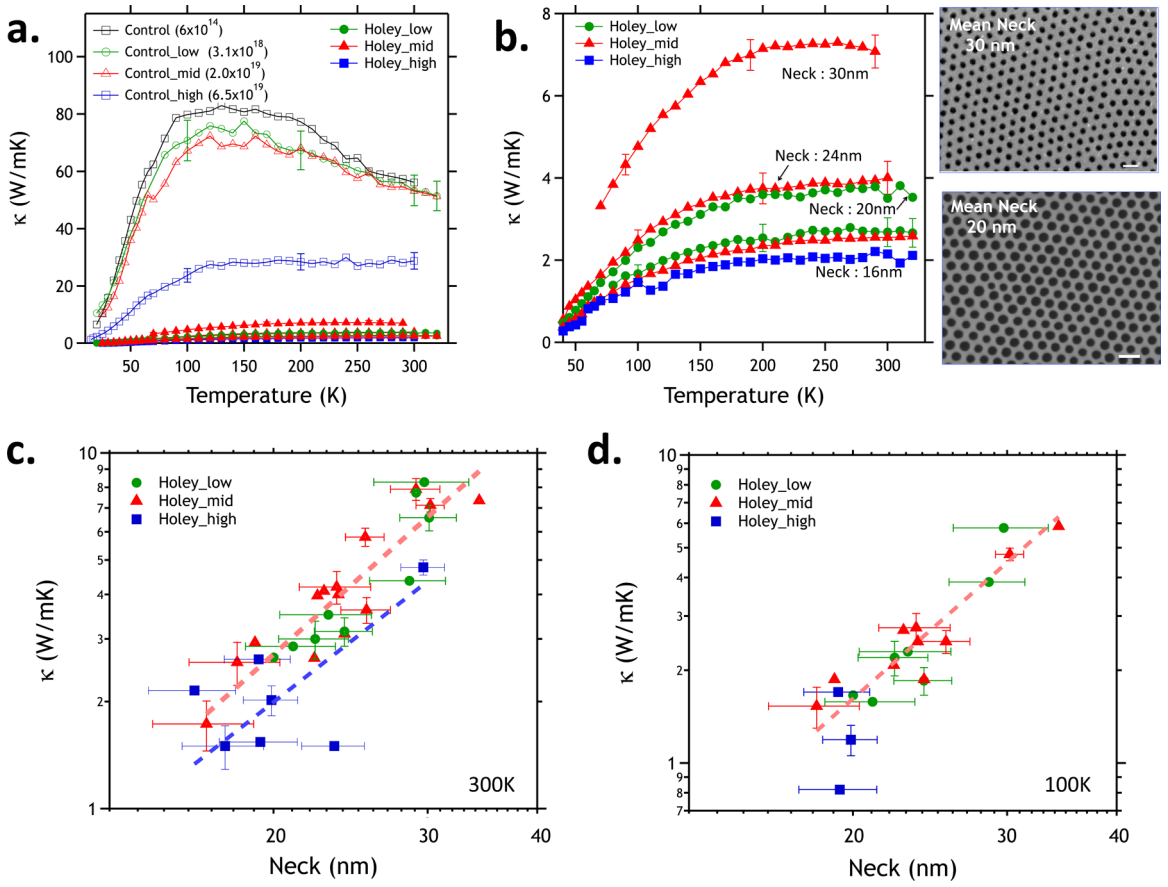

Figure 4. Thermal conductivities of the control silicon ribbons and HS ribbons with different doping levels (boron-doped): 3.1×10^{18} cm^{-3} (green circles), 2.0×10^{19} cm^{-3} (red triangles), and 6.5×10^{19} cm^{-3} (blue squares). Open circles, triangles, and squares are for control silicon ribbons. Solid circles, triangles, and squares are for HS ribbons. (a) Temperature-dependent thermal conductivities of control silicon and HS ribbons with varied doping concentrations. (b) Temperature-dependent thermal conductivities of HS ribbons, which is the enlarged illustration of (a). The mean neck sizes were estimated based on SEM images as shown. Scale bars are 100 nm. (c) HS thermal conductivities, at 300 K, as a function of the neck size for different doping levels are plotted in log−log scale. The power law fittings are guidelines for the thermal conductivity of low- and mid-doped HS ribbons combined (dashed red line) and for high-doped HS devices (dashed blue line), respectively. (d) Plot of HS thermal conductivity, at 100 K, *vs* neck size for different doping levels. The power law fitting is provided as a guideline (dashed red line).

through the HS ribbon was obtained by measuring the temperature difference (ΔT) between hot and cold PRT pad, in which HS's thermal conductance was calculated. During the ΔT measurement, an open-circuit voltage across a HS ribbon (*i.e.*, the Seebeck voltage) was also measured between the two inner ohmic contacts, which provided the Seebeck coefficient ($S = -\Delta V/\Delta T$). We noticed that Seebeck voltages measured by either inner or outer contacts were comparable and within the measurement of uncertainty. Our run-to-run measurement variance of Seebeck voltage is less than 10%. For HS ribbons, ribbon dimensions and neck/pitch sizes of holey arrays were measured by SEM. HS porosities, φ, were then considered in the calculations of thermal conductivity and electrical conductivity. As revealed by TEM (Figure 2b, inset), the surface oxide thickness is 1−2 nm, resulting an uncertainty of HS's solid thermal conductivity and electrical conductivity, approximately 10−15%. We assume a worst-case scenario that there is no thermal conduction through 2 nm thick oxide. Consequently, for 20 nm neck and 60 nm pitch HS, the solid thermal conductivity would increase by 15%, from 2.7 to 3.1 W/mK, which is still within the uncertainty of our measurement. Detailed measurements using fully integrated microdevices could be found in the Supporting Information.

In order to investigate the HS size effect, we applied the same BCP array and carefully controlled the neck size by modulating deep reactive ion etching (DRIE) parameters and the HS etching mask (*i.e.*, Cr) thickness. As shown in Figure 3, uniform hole diameters across Si films could be routinely reproduced. Figure 4a,b presents the temperature-dependent thermal conductivities of the control ribbons and the representative HS ribbons, with low- (3.1×10^{18} cm^{-3}), mid- (2.0×10^{19} cm^{-3}), or high-doping (6.5×10^{19} cm^{-3}) concentrations (all acquired by four-point probe resistivity measurement). The thermal conductivities of control silicon ribbons match well with the values of in-plane thermal conductivity of silicon thin films reported in the literature,[27−29] which validates the measurements of this work. This is due to an improved accuracy provided by our integrated microdevices. The covalent contact between silicon and SiN_x (in the PRT end pad) has a negligible parasitic thermal contact resistance, which is also demonstrated by Hippalgaonkar *et al.*[30]

The Matthiessen's rule suggests the total relaxation time can be described as $\tau^{-1} = \tau_U^{-1} + \tau_{imp}^{-1} + \tau_B^{-1}$, where the subscripts U, imp, and B refer to Umklapp, impurity, and boundary scattering, respectively. In Figure 4a, there is only a small reduction in thermal conductivity at 300 K (less than 10%) from light- ($\sim 6 \times 10^{14}$ cm^{-3}), to low- (3.1×10^{18} cm^{-3}), and to mid-doped (2.0×10^{19} cm^{-3}) control samples, which suggests that the total

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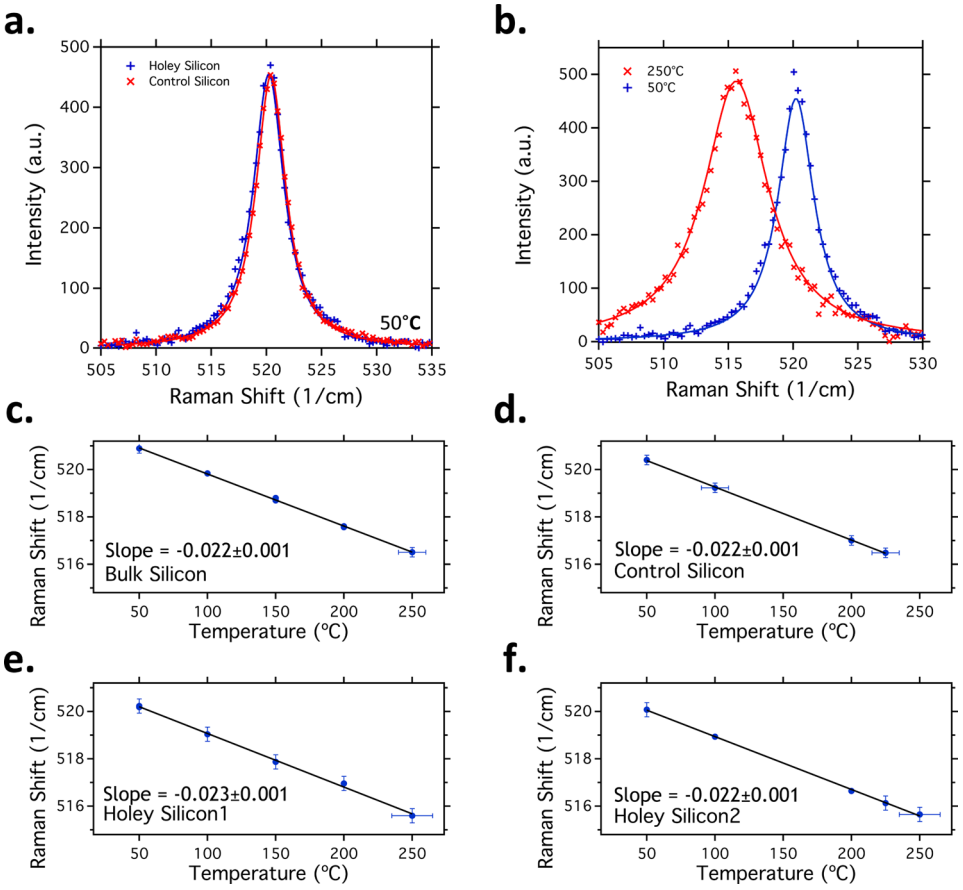

Figure 5. (a) Raman spectroscopy data at 50 °C. The full width at half-maximum is 3.33 cm^{-1} for holey silicon and 3.27 cm^{-1} for the control silicon ribbon. Their difference is within the measurement uncertainty.[35] Reprinted with permission from ref 35. Copyright 2015 American Chemical Society 2015. (b) Raman spectra of HS at 50 and 250 °C. Peak is red-shifted and broadened with temperature. (c–f) Raman peak position as a function of temperature, and the slopes are 0.022 ± 0.001, 0.022 ± 0.001, 0.023 ± 0.001, and 0.022 ± 0.001 cm^{-1}/K for bulk silicon, control silicon, holey silicon 1, and holey silicon 2, respectively. The changes in the slopes are within the measurement of uncertainty.

relaxation time is dominated by the phonon boundary (100 ± 10 nm in ribbon thickness) and the Umklapp scattering, as opposed to impurity scattering. We performed the nongray Boltzmann transport equation (BTE) model to fit our experimental data (available in Supporting Information) and found a good agreement with previous literature,[27−29] confirming a comparable role of the impurity scattering in low- and mid-doped samples. Yet, the thermal conductivity of the high-doped (6.5×10^{19} cm^{-3}) control ribbon decreases to nearly one-half of the value of the low- and mid-doped control ribbons. The greatly suppressed thermal conductivity at the high-doping level (>6×10^{19} cm^{-3}) was also previously reported and attributed to unintentional impurities.[27,29,32] In our case, the total impurity (*i.e.*, boron dopants) concentration is ~4×10^{20} cm^{-3} for the high-doped sample based on the implantation dose (the calculated doping profile is available in Supporting Information), and only a part of dopants could be activated by the post-annealing process, yielding a carrier concentration of 6.5×10^{19} cm^{-3}. Considering the total impurity concentration, our BTE calculation yielded a good agreement with measured thermal conductivity, suggesting a key role of the high dopant concentration in such a low thermal conductivity. Additionally, impurity modeling by the SRIM (stopping and range of ion in matter) package (available in Supporting Information) indicates that, in addition to boron impurities, an ion implantation process would induce defects of silicon vacancies and interstitials.[31] As the post-annealing only partially repaired these defects, resulting in relatively higher concentrations of these defects, their contributions to phonon scattering are significant in high-doped samples.

The temperature-dependent thermal conductivities of the representative HS ribbons were dramatically reduced for all three doping concentrations, which is consistent with the earlier BCP-patterned HS.[10] Figure 4b shows that smaller necks result in a flatter temperature dependency, and the Umklapp peak in $\kappa(T)$ is absent due to a faster phonon boundary scattering rate.[11] For HS, the neck size can be considered as the limiting dimension for phonon transport. In a similar case, the diameter of silicon nanowires is the limiting dimension for phonon transport. Interestingly, the thermal conductivity of HS is much lower than that of smooth nanowires, with diameters comparable to HS necks. For example, nanowires with a diameter of 37 nm have a $\kappa \sim 17$ W/mK; nanowires with a diameter of 22 nm have a $\kappa \sim 7$ W/mK.[33] Yet, surface to volume ratios of our HS samples (0.09 and 0.14 nm^{-1} for HS with a neck size of 37 and 22 nm, respectively) are actually smaller than those of nanowires (0.11 and 0.18 nm^{-1} for nanowires with a diameter of 37 and 22 nm, respectively). The cross-sectional SEM images (see Figure 3) and high-resolution TEM image (see Figure 2b, inset) both indicate that hole sidewall surfaces are relatively smooth, and thus the roughness effect, that occurs in rough nanowires,[9,12] may not play a dominant role in reduction of thermal conductivity.

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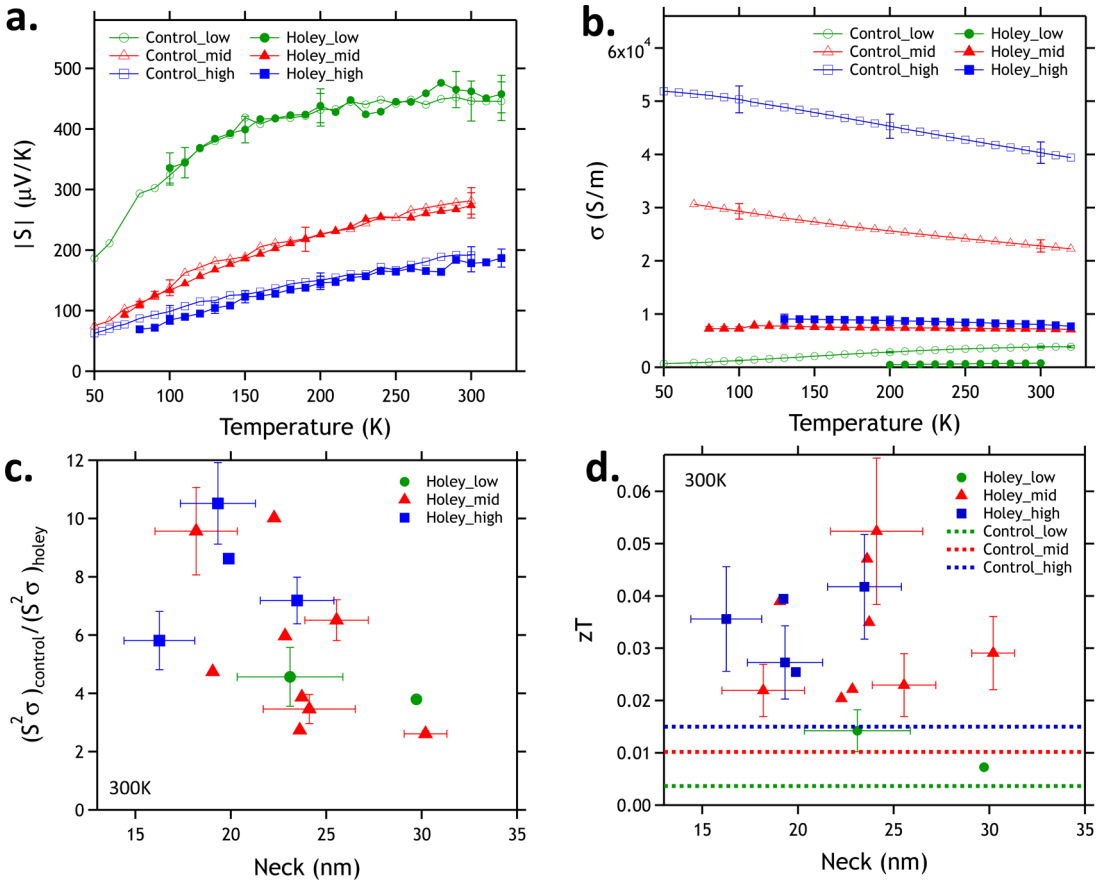

Figure 6. Temperature-dependent (a) Seebeck coefficient and (b) electrical conductivity. The neck sizes are ~23, ~24, and ~16 nm for low-, mid-, and high-doped HS devices, respectively. (c) Power factor comparison of HS ribbons with control ribbons. (d) *zT* plot of the HS ribbons with respect to the neck size at 300 K. The *zT* of control silicon ribbons (dashed lines) are provided for a comparison.

One possible reason for the lower thermal conductivity of HS is that the fraction of phonon backscattering at the sidewalls of the holes is significantly larger than that of smooth nanowires. Based on the MC simulations of Moore *et al.* and Ravichandran *et al.*,[24,34] 50% of the incident phonons are backscattered at nanowire surfaces that are aligned parallel to the temperature gradient. Accordingly, the sidewall surfaces of HS, perpendicular to the temperature gradient, would backscatter more than 50% of incident phonons, resulting in a lower thermal conductivity in the holey structure.

In order to confirm crystal quality and lattice anharmonicity, we performed Raman spectroscopic measurements for HS and control silicon ribbons. As shown in Figure 5a, it is clearly shown that there is no significant difference in Raman peak shift and full width at half-maximum (fwhm) between HS and the control silicon ribbon, suggesting that our HS does not have considerable defect clusters or nanocrystalline domains after DRIE etching.[35−37] We further performed temperature-dependent Raman spectroscopic measurements, from 50 to 250 °C, for both HS and the control silicon ribbon, as shown in Figure 5b. The Raman peaks red shift and broaden with temperature due to thermal expansion and anharmonic phonon−phonon coupling.[38] The slope of frequency *versus* temperature can be approximately expressed with a lattice expansion and an anharmonicity contribution as[39]

$$\left(\frac{d\omega}{dT}\right) \approx -3\omega_o\gamma\alpha + \frac{k_B}{hc\omega_o}[4A + 9B]$$

where γ, α, A, and B are the Grüneisen parameter, coefficient of linear thermal expansion, the cubic, and quartic anharmonic constants, respectively. Shown in Figure 5c−f, the slopes are -0.022 ± 0.001, -0.022 ± 0.001, -0.023 ± 0.001, and -0.022 ± 0.001 cm^{-1}/K for bulk silicon, the nonholey control ribbon, HS ribbon 1, and HS ribbon 2, respectively. Since there is no significant difference among these samples, our data indicate that lattice anharmonicity of HS is the same as that of the bulk and control silicon ribbon. Therefore, neither crystal defects nor lattice anharmonicity is a source of thermal conductivity reduction in HS.[39]

To uncover the impact of incoherent phonon boundary scattering, the neck size effect is carefully analyzed and the results are plotted in Figure 4c,d. It is shown that the neck size in the range of 16−34 nm impacts phonon transport greatly at 100 and 300 K. Specifically, the HS thermal conductivity at 300 K decreases from 7.2 ± 0.7 to 1.8 ± 0.2 W/mK, as the neck decreases from 34 to 16 nm. It is also noticeable in Figure 4c that the thermal conductivity of HS is nearly independent of the doping level, which indicates that the phonon boundary scattering plays a more dominant than the impurity scattering in the κ reduction. It was demonstrated earlier that phonons with MFP longer than 20 nm would account for approximately 97% of the total heat conduction in bulk silicon,[40] and the strong phonon boundary scattering (*i.e.*, necking effect) in BCP-patterned HS was found.[10] Empirically, a correlation could be captured using a power law fit, $\kappa = a \times \text{neck}^n$,[41] where a and n are only fitting constants. The size-dependent scaling factor (n) is

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found to be ~2 in contrast to the $n \sim 1$ trend in the nanowire system.[33,41,42] Such a $n \sim 2$ correlation might result from various effects in HS samples, including coherent phonon transport (zone folding), particle regime (phonon backscattering), and elastic modulus change. For example, the strong reduction of thermal conductivity and $n = 2-3$ dependency was found in the theoretical result of Dechaumphai *et al.* because of a partial coherent phonon effect.[25] In addition, the elastic softening effect due to a surface dangling bond and surface stress could solely result in $n = 2-3$, as recently found in a thin crystalline silicon nanotube (tube wall thickness = 5−10 nm).[43] In our HS, the neck size is clearly larger than the thickness of silicon nanotube wall, and the elastic softening effect remains to be investigated. Also, applying coherent transport to a BCP-patterned HS structure needs further validation, a point which we will return to later. By considering all respects as described above, more studies are necessary to further investigate the relation between a scaling factor and each effect.

MC and BTE calculations considering the classical particle regime found the lowest thermal conductivity of the HS system with the same neck/pitch dimension, approximately 8−10 W/mK.[24,25] The predicted values can be considered as the Casimir limit,[44] and they clearly disagree with the experimental data presented here. This raises again the question about the possibility of coherent phonon transport in the nanolithography-fabricated HS. Here, we demonstrated that by keeping the HS pitch while reducing the neck size, the increased surfaces from the increased hole sizes are shown to be effective at greatly reducing the thermal conductivity. Indeed, coherent phonon transport can potentially occur when they meet the following condition.[45−47] Phonons with longer MFP than the neck size scatter specularly at pore boundaries and retain their phase information over multiple periods of pores. As a result, the interference of these phonons intervened by a periodic hole array modifies phonon dispersion relation and group velocity. It is expected that long wavelength phonons scatter in HS more specularly than ones with short wavelengths,[35] but the exact cutoff frequency between incoherent and coherent phonons is still unclear, as pointed out in respective simulation works.[24,25] For instance, Dechaumphai *et al.*'s calculation set the cutoff frequency at ~4THz and acquired the ultralow thermal conductivity of HS based on a coherent scattering effect.[25] Additionally, our HS samples have imperfections in the holey array, such as line and point defects induced during the BCP assembly process, and the resultant neck/pitch size also has ~2 nm error width.[35] These variations in periodicity may disturb the coherent interference especially for short wavelength phonons. Thus, it may be needed to fabricate HS with a true periodicity (likely can be provided by e-beam lithography but not the BCP approach used here) and a pitch size on the order of a few nanometers or less, in order to efficiently interfere with phonons with terahertz frequency at room temperature.[23,24]

The electrical properties of each HS ribbon were characterized accordingly, and their thermoelectric performances were obtained. Figure 6a shows the Seebeck coefficients of HS ribbons and control ribbons with the three doping concentrations. The room temperature Seebeck coefficient of low-, mid-, and high-doped HS ribbons are 470 ± 32, 270 ± 22, and 197 ± 14 μV/K, respectively. They are very comparable with those of low-, mid-, and high-doped control silicon ribbons: 446 ± 31, 280 ± 21, and 190 ± 15 μV/K. The unchanged Seebeck coefficients in HS suggest that there is no detectable variance in the electronic band structure after the addition of the periodic hole arrays. As shown in Figure 6b, the electrical conductivity was adversely affected by the holey structure, and thus the corresponding power factors were reduced (Figure 6c). The undesired reduction in the electrical conductivity is due to the fact that the native oxide poorly passivates the HS surfaces. When large surface areas were created in HS samples, high surface charge density with positive charged polarity was possibly created, which in turn inducesd a depletion layer to reduce the conduction channel within boron-doped HS.[48] While surface states could be removed by forming a thin thermal oxide (COMS-grade gate oxide), the metalized electrical contact in our microdevices would not survive in the oxidation temperature (800−1000 °C). Instead, we passivated HS with a 3−5 nm thick Al_2O_3 layer by atomic layer deposition (ALD), followed by annealing at 500 °C in H_2 (10%)/Ar (90%) for 30 min. It is known that the ALD Al_2O_3 layer with fixed negative charges can provide effective field-effect passivation for p-type silicon and thus decreases the surface defect density.[49−51] As a result, the electrical conductivity increased by ~30% for the mid-doped HS (data available in Supporting Information).

High concentration of defects, such as silicon vacancies, silicon interstitials, and boron impurities, might be induced by ion implantation and was assessed *via* the SRIM model (available in Supporting Information).[31] We noticed that, for the control samples, the electrical conductivities after the rapid thermal activation were lower than the predicted values (by Profile Code, available in Figure S1 in Supporting Information). We estimated that for low-, mid-, and high-doped samples, the carrier concentrations are 52, 23, and 16% of the expected carrier concentrations. This suggests that remaining defects, including inactivated boron (as interstitial impurities), silicon vacancies, and silicon interstitials, are still prevailing in these control samples and HS samples.

Despite the fact that the electrical conductivity was reduced, it is shown in Figure 6d that the zT can be enhanced by up to 5 times as compared with the control Si ribbons. The opposing trends in the neck-size-dependent thermal conductivity and power factor dictate an optimal neck size for an optimized zT value for our HS samples. Specifically, the zT enhancement could lead to values as high as 0.05 at room temperature for HS samples with a neck size of 24 nm and a doping level of 2.0×10^{19} cm^{-3}. Such a zT value is lower than that of the HS samples in the previous report (~0.4 at 300 K),[10] where the HS samples were doped using diffusion instead of ion implantation. The selection of ion implantation in this work is due to the compatibility with the microfabrication process. Yet, zT values in our monolithic HS system are limited by electrical conductivity that is caused mainly by ion implantation defects and surface defects. It is possible that higher zT values can be further acquired by optimizing several aspects, such as doping using thermal diffusion to prevent the ion implantation defects, eliminating surface dangling bonds by a high-temperature dry oxidation, and reducing the neck/pitch size of the holey structure to further reduce thermal conductivity.

CONCLUSIONS

We have fabricated fully integrated microdevices that allow measuring thermal conductivity, electrical conductivity, and the Seebeck coefficient for the same HS ribbon. The HS was patterned by BCP lithography to yield a significantly reduced thermal conductivity below the Casimir limit. Raman analysis confirmed neither defect clusters nor lattice anharmonicity is a source of thermal conductivity reduction in HS. Using fully integrated microdevices, the impact of incoherent phonon

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scattering in HS was experimentally correlated by systematically varying the neck size. Further, the optimal thermoelectric performance of the HS system was assessed as a function of doping level and neck size over 20 devices. Finally, for practical thermoelectric device fabrication, we would suggest diffusion-based doping over ion implantation to avoid unintentional defects, such as vacancies, silicon interstitials, and inactivated impurities. Also, a surface oxide layer for hole wall passivation should be grown by a dry oxidation process at high temperature (800−1000 °C) before metallization for electrical contact is made. These data will help shed light on future silicon-based thermoelectric devices and also help advance the fundamental understanding of complex phonon transport mechanism in the HS system.

METHODS

Control Silicon Microdevices. The microdevice fabrication was carried out using the standard 4 in. microfabrication technique, including nine photolithography steps, one ion implantation, six dry etching processes, two wet-etching processes, one chemical vapor deposition of low-stress SiN_x, two metallizations, and one critical point drying. The 4 in. prime silicon-on-insulator (SOI) wafers were purchased from Soitec, and the ion implantations were conducted at Core Systems. The end-of-line yield of working devices was nearly ∼95%, which was limited by the process of releasing control silicon microdevices from the SOI wafers. Details of the control silicon microdevice fabrication are available in the Supporting Information.

Holey Cr Mask. A poly(styrene-*block*-2-vinylpyridine) (PS-*b*-P2VP) copolymer with molecular weight of 183.5 kg/mol (M_n^{PS} = 125 kg/mol; M_n^{P2VP} = 58.5 kg/mol) and the molecular weight distribution of 1.05 was spun on the SiO_2(300 nm)/Si substrate, followed by solvent annealing for approximately 3 h to enhance the lateral order of the micellar array.[52] This highly ordered film was soaked in ethanol for 30 min to produce holes with a diameter of several tens of nanometers. A thin Cr mask was formed on the reconstructed BCP film by e-beam evaporation with a tilted angle of 75°, so that Cr would be deposited on the film surface but not block the holes of the BCP patterns. To detach the Cr holey mask from the SiO_2/Si substrate, the Cr holey mask was first protected with an additional layer of BCP film, and then it was immersed in a <3% (vol %) dilute HF bath to etch off SiO_2 underneath of the Cr holey mask. Details of the BCP process are available in the Supporting Information.

HS Microdevices. HS microdevices were fabricated by inserting an additional BCP/DIRE process to fabricate the control silicon microdevice. The freestanding Cr holey mask was transferred to a prefabricated microdevice chip (1 × 1 cm), and oxygen plasma was applied to strip off the BCP films, leaving the holey Cr mask. The HS was fabricated by DRIE etching silicon through the Cr holey mask. After the DRIE process, the Cr holey mask was etched away by a commercial Cr etchant, CR-7, for 1 min. Finally, to suspend the HS microdevice, the DRIE was performed to etch through the handle wafer (∼450 μm), and the fluorocarbon-based dry etching (CHF_3/Ar = 80/4 sccm, 150 W) was then applied to etch off the buried oxide. The etching end-point was determined by the oxide color *via* an optical microscope and also confirmed by SEM. The end-of-line yield, ∼30%, was achieved, where the reduced yield was due to the holey structure. Details of the HS microdevice fabrication are available in the Supporting Information.

Characterizations. The microdevices were examined by optical microscopy (Leica INM100), scanning electron microscopy (SEM, JEOL JSM 6340F), transmission electron microscopy (TEM, Tecnai FEI), and Raman (HORIBA LabRAM HR Evolution).

ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge on the ACS Publications website at DOI: 10.1021/acsnano.5b05385.

Experimental details including ion implantation process (including Profile Code simulation), fabrication of HS, simultaneous thermoelectric property measurements, Al_2O_3 passivation, Raman experiment, BTE models for control samples, and defect assessments using SRIM (PDF)

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Notes

The authors declare no competing financial interest.

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