Supporting Information for:

Low-Temperature Solution-Phase Growth of Silicon and Silicon-Containing Alloy Nanowires

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Figure S8. Relationship between nanowire diameter and precursor concentration.

Figure S9. Relationship between nanowire diameter and reaction temperature.

Figure S1. Ga-Si binary phase diagram (see: Olesinski, R. W.; Kanani, N.; Abbaschian, G. J. *Bull. Alloy Phase Diagr.* 1985, 6, 362-364).
Figure S2. Powder X-ray diffraction (XRD) pattern of Si nanowires synthesized using triethylgallium and tris(trimethylsilyl)silane precursors in hexadecane at 274 °C (red). The standard pattern of cubic Si (black bars; JCPDS no. 27-1402) is also shown for comparison.
Figure S3. TEM image of Ga-catalyzed Si nanowires synthesized using triethylgallium and tris(trimethylsilyl)silane precursors in hexadecane at 210 °C. As indicated by the result, the morphology and quality of the resultant nanowires are not as good as those grown at its optimized condition (around 280 °C). The possible reason that lower temperature results in low-aspect-ratio nanowires is that the continuous decomposition of the silicon precursor at the surface of the Ge nanodroplets could not be maintained when the temperature is too low.
Figure S4. (a) Zero-loss peak (ZLP) of a monochromated electron beam in TEAM 1 with Schottky field-emission source. The energy spread of a monochromated ZLP was ~100meV in full-width at half-maximum (FWHM). The energy dispersion was 0.01eV/ch. The camera length was 29.5mm and the entrance aperture of the GIF system was 2.5mm in diameter. The convergence and collection angles are 26mrad and 39mrad, respectively. Low voltage (80kV) VEELS was applied aiming at improving the energy resolution and decreasing the delocalization of the energy loss, while minimizing the relativistic effects. (b) Demonstration of the ZLP background removal using a power-law subtraction. (c) Bandgap value was obtained by fitting the intensity onset with $(E-E_g)^{3/2}$ type function.
Figure S5. TEM image of Si_{x}(GaP)_{y} nanowires synthesized using triethylgallium, tris(trimethylsilyl)phosphine, and trisilane precursors in hexadecane at 180 °C.
Figure S6. Si percentage obtained by EDS analysis along the length of a single Si$_x$(GaP)$_{1-x}$ nanowire synthesized using triethylgallium, tris(trimethylsilyl)phosphine, and trisilane precursors in hexadecane at 180 °C.

Figure S7. The relationship between silicon content in the as-grown alloy and the relative ratio of starting GaP and silicon precursors using triethylgallium, tris(trimethylsilyl)phosphine, and
trisilane precursors in hexadecane at 180 °C. The silicon content in the as-grown alloy nanowires is highly dependent on the relative ratio of starting GaP and silicon precursor. Typically, the more silane added (higher silane precursor ratio), the more silicon content in the alloyed nanowires. Also, it is worth to note that the distribution of silicon and GaP along the nanowire follows similar pattern where GaP is more favorable at the beginning of the reaction while silicon is more favorable towards the end of nanowire growth.

Figure S8. Nanowire diameters increase as precursor concentration increases when using triethylgallium, tris(trimethylsilyl)phosphine, and trisilane as precursors.
Figure S9. Nanowire diameters decrease as reaction temperature increases when using triethylgallium, tris(trimethylsilyl)phosphine, and trisilane as precursors.