Supporting Information (SI)

Simultaneous Thermoelectric Property Measurement and Incoherent Phonon Transport in Holey Silicon

Jongwoo Lim,[#,1,2] Hung-Ta Wang,[#,1,3] Jinyao Tang,[1,4] Sean C. Andrews,[1,2] Hongyun So,[5] Jaeho Lee,[1,6] Dong Hyun Lee,[7,8] Thomas P. Russell,[8] and Peidong Yang[1,2,9,10]*

[1]Department of Chemistry, University of California, Berkeley, California 94720, United States

[2]Materials Sciences Division, Lawrence Berkeley National Laboratory, Berkeley, California 94720, United States

[3]Department of Chemical and Biological Engineering and Center for Materials for Information Technology, University of Alabama, Tuscaloosa, Alabama 35487, United States

[4]Department of Chemistry, The University of Hong Kong, Hong Kong

[5]Department of Mechanical Engineering, University of California, Berkeley, California 94720, United States

[6]Department of Mechanical and Aerospace Engineering, University of California, Irvine, California 92697, United States

[7]Department of Polymer Science and Engineering, Dankook University, 126 Jukjeon-dong, Suji-gu, Yongin-si, Gyeonggi-do, 448-701, Korea.

[8]Department of Polymer Science and Engineering, University of Massachusetts, Amherst, MA 01003, United States

[9]Department of Materials Science and Engineering, University of California, Berkeley, California 94720, United States

[10]Kavli Energy Nanosciences Institute, Berkeley, California 94720, United States

#: These authors contributed equally to this work

*: Author to whom correspondence should be addressed. E-mail: p_yang@berkeley.edu

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1. SOI Samples

The 4" prime silicon-on-insulator (SOI) wafers were purchased from Soitec. The (100) device layer is boron-doped (14-22 $\Omega \bullet$cm) and with a thickness of 340 ± 6 nm. The buried oxide is 1000 ± 22.5 nm in thickness, and the (100) handle wafer is boron-doped (14-22 $\Omega \bullet$cm), 450 ± 10.0 μm in thickness.

2. Ion Implantation

To obtain a uniform cross-plane carrier doping profile, the ion implantation samples were designed to have ~100 nm device layer with a capping layer of ~50 nm silicon dioxide. The fabrication processes for preparing ion implantation samples were performed in UC Berkeley Microfabrication Laboratory or Marvell Nanofabrication Laboratory. We first thinned down the device layer to ~120 nm by the wet oxidation (O_2=10 SLM, 1000°C, 1 hour and 43 minutes, by tystar2), followed by a hydrofluoric acid (HF) etch. A dry oxide film (thickness= 51 ± 2.0 nm) was then grown (O_2=10 SLM with 3 ml/min de-ionized (DI) water, 1000°C, 1 hour and 2 minutes, by tystar2) as the capping layer for the ion implantation. After the above two oxidation processes, the thickness of the device layer (*i.e.*, the silicon ribbon thickness) is confirmed as 98 ± 3.4 nm across the entire 4" wafer and among the seven wafers, which was characterized by the spectrometer (nanospec) and the profilometer (asiq).

As shown in **Figure S1**, the doping profiles were predicted using the commercial simulator, Profile Code. The ion implantations were conducted at Core Systems, and the implantation doses (conditions) are: 5.0×10^{13} cm^{-2} Boron (31 keV, titled 7°), 5.0×10^{14} cm^{-2} Boron (31 keV, titled 7°), and 5.0×10^{15} cm^{-2} Boron (31 keV, titled 7°), respectively. The rapid thermal annealing (heatpulse4) was applied to activate the dopants. The actual rapid thermal annealing condition was tested to be 45s at 1050 °C in N_2 for acquiring the highest carrier concentrations. The four-point resistivities (4ptprb) were measured, and the carrier concentrations were back calculated as 3.1×10^{18} cm^{-3}, 2.0×10^{19} cm^{-3}, and 6.5×10^{19} cm^{-3}, respectively, which are less than the expected values of 4.0×10^{18} cm^{-3}, 4.0×10^{19} cm^{-3}, and 4.0×10^{20} cm^{-3} (see dopant profiles after thermal activation in **Figure S1**). The obtained carrier concentrations are below the predicted values as expected, possibly owing to damages created by the ion implantations and an incomplete activation, as shown later in the SRIM simulations.

a.
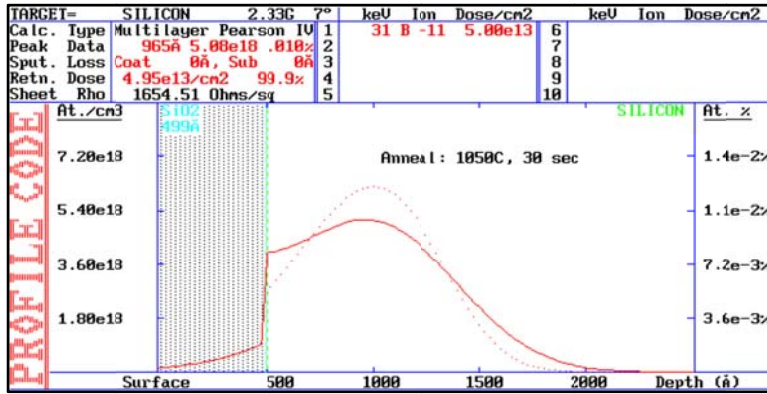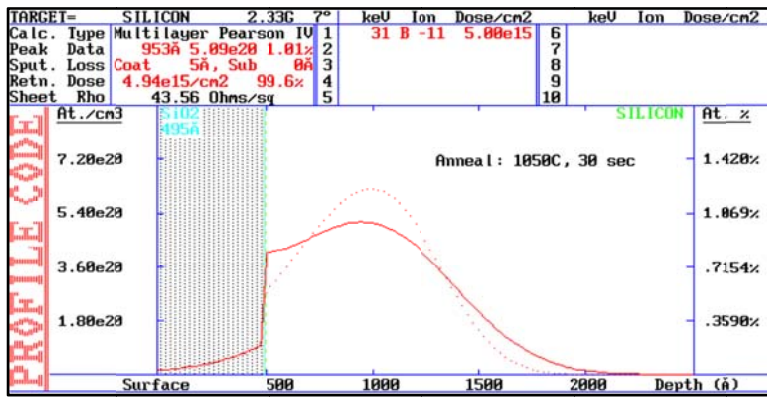

b.
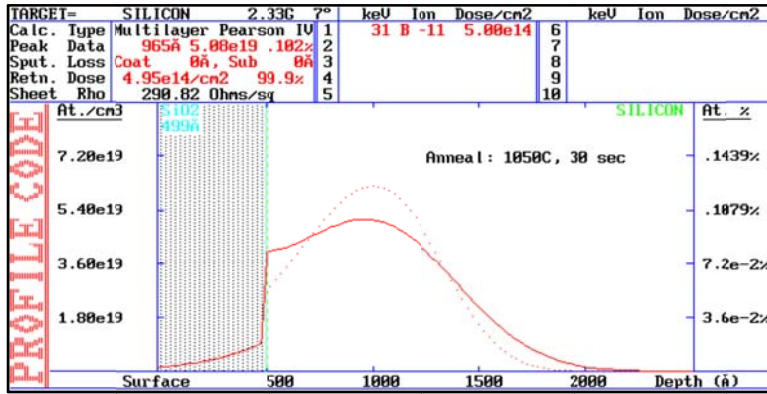
c.

Figure S1. The predicted doping profiles, before (red solid line) and after (red dot line) thermal activation (1050°C for 30s), are shown for **(a)** low-boron, **(b)** mid-boron, and **(c)** high-boron, respectively.

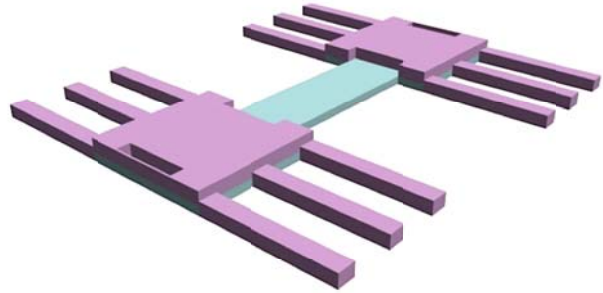## 3. Fabrication of Control Silicon Ribbon Microdevices

The fabrication processes for the microdevices were performed in UC Berkeley Microfabrication Laboratory and Marvell Nanofabrication Laboratory, except that the low-stress silicon nitride (SiN_x) was grown using Stanford Nanofabrication Facility. The fabrication processes were carried out using the standard 4" microfabrication processes, including nine photolithography steps, six dry etching processes, two wet-etching processes, one chemical vapor deposition of low-stress SiN_x, two metallization processes, and one critical point drying. **Figure S2** shows the schematic of the microdevice at the four fabrication stages. Frist, the silicon ribbon dimension, including silicon ribbon length and width, was defined using the photolithography (gcaws2), and we performed the deep reactive ion etching (DRIE; 2 cycles of passivation/etching by STS. For passivation: C_4F_8= 100 SCCM, 600 W, 7 seconds; for etching: SF_6/O_2=130/10 SCCM, 600 W, 9 seconds) to tailor the silicon ribbon and the two end-pads, as shown in **Figure S2(a)**. The ~300 nm-thick low-stress SiN_x, required for suspending the microdevice, was then deposited (SiH_2Cl_2/NH_3=100/25 SCCM, 140 mTorr, 835°C, 90 minutes, by tylannitride at Stanford). The covalent bonding between low-stress SiN_x and silicon end-pads results in a low thermal resistance at the SiN_x/Si interface, and consequently the accuracy of the thermal conductivity measurement was greatly improved. This improvement is particularly important for measuring thermal conductivity of control silicon ribbons due to their low thermal resistance. We performed the reactive ion etching (CHF_3/CF_4=30/90 SCCM, 100W, 250~400 seconds, by ptherm), followed by a HF etch, to etch away SiN_x on the top of the silicon ribbon and to open the four windows for the four-point ohmic contacts; the microdevice at this stage is illustrated by **Figure S2(b)**. Chromium/Platinum (Cr/Pt = 2/40 nm, by ultek) was then e-beam evaporated to make contacts to the silicon ribbon. Cr/Pt (2/30 nm, by edwards) was sputtered to make the platinum resistance thermometers (PRT). The rapid thermal annealing (630 °C for 30s, by heatpulse2) was conducted to form the ohmic contacts to the silicon ribbon. The microdevice was then patterned (gcaws2) and subjected to the reactive ion etching (CHF_3/CF_4=30/90 SCCM, 100W, 600 seconds, by ptherm) to form the two PRT pads (*i.e.*, the SiN_x/Si end-pads) by etching away low-stress SiN_x at the un-wanted areas. The microdevice for the control silicon ribbon was nearly completed except that the microdevices were still attached to the SOI substrate.

To release the control silicon ribbon microdevices from the buried oxide and the handle wafer, the back-side etching windows were defined by the photolithography (ksaligner) and the reactive ion etching (CHF$_3$/CF$_4$=30/90 SCCM, 100W, 600 seconds, by ptherm) was performed to etch away SiN$_x$ to open the etching windows. For the through wafer etching (*i.e.*, the releasing process), the 4" wafers were first diced into 8×8 mm-sized chips (as shown in **Figure S5(a)**), consisting of 72 silicon ribbon microdevices. The thick photoresist (SPR-220, 1800 rpm, hot-baked at 120°C for 30 mins) was used as the etching mask, and the etching window was reopened by the photolithography (ksaligner). Prior to the through wafer etching processes, the front-side of the chip (*i.e.*, the device side) was coated with regular photoresist (g-line, OCG 825 35CS) to protect the silicon ribbons, and the chip was then bonded, back-side up, to a 4" handle wafer. To fully etch away the 450 μm-thick handle wafer of the SOI sample, we performed the DRIE (565 cycles of passivation/etching by sts, For passivation: C$_4$F$_8$= 100 SCCM, 600 W, 7 seconds; for etching: SF$_6$/O$_2$=130/10 SCCM, 600 W, 9 seconds). To etch way the buried oxide of the SOI sample, we then performed the fluorocarbon-based dry etching (CHF$_3$/Ar=80/4 SCCM, 150W, by ptherm) with the high etching selectivity (SiO$_2$:Si > 30:1) and the ultra slow etching rate (20 nm / min for SiO$_2$). Finally, the microdevices were finally suspended by dissolving the protective photoresist in a both of the commercial photoresist stripper (PRS-3000, 80°C for 12 hours), and then dried in carbon dioxide critical fluid (cpd2). A released control silicon ribbon microdevice is illustrated in **Figure S2(c)**.
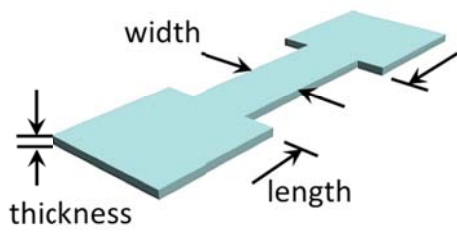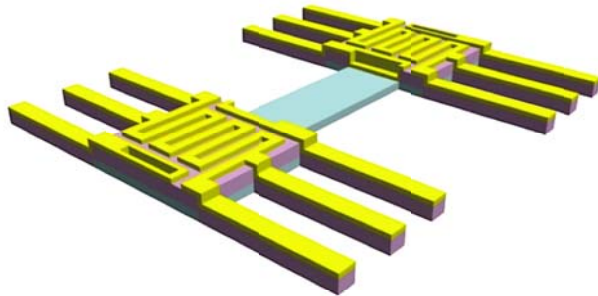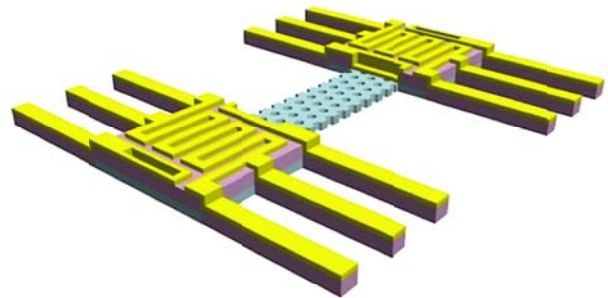
**Figure S2.** Schematic of the microdevice fabrication.

## 4. Fabrication of Holey Silicon Ribbon Microdevices

For holey silicon (HS) ribbon microdevices, we developed a scalable nanolithography process based on block copolymer (BCP) assembly, as shown in **Figure S3**. A poly(styrene-*block*-2-vinylpyridine) (PS-*b*-P2VP) copolymer with molecular weight of 183.5 kg mol^{-1} (M_n^{PS}=125 kg mol^{-1}; M_n^{P2VP}=58.5kg mol^{-1}) and molecular weight distribution of 1.05 was spun on 300 nm-thick silicon oxide substrates, followed by a vapor phase toluene annealing for approximately 3 hours to enhance the lateral order of the micellar array. The highly ordered film was soaked in ethanol for 30 minutes to produce nanometer-sized pores by reconstructing the P2VP regions because ethanol was a selective solvent to P2VP chains. A thin Cr film was deposited using e-beam evaporation (ultek) on the reconstructed BCP film with a 75 degree tilt, by which Cr could not block the holes of the BCP patterns, and consequently a Cr holey mask was made.

To transfer the Cr holey mask from the oxide chip to the chip with the pre-fabricated microdevices, the Cr holey mask was first protected with an additional layer of BCP film, and then the chip was slowly dipped in a dilute HF (<3%) bath. When the 300 nm thick SiO_2 was quickly etched away, the protected Cr holey mask floated on the surface of the aqueous bath due to its hydrophobicity, as shown in **Figure S4**. The floated Cr holey mask was rinsed and picked up by the chip with pre-fabricated microdevices. We then applied oxygen plasma to remove the BCP film, leaving the holey Cr mask for the following DRIE etching for fabricating HS. We could control the neck width (or porosity) of the HS by tuning the DRIE etching parameters and the Cr mask thickness. After the DRIE, the Cr holey mask was etched away by dipping the device chip in a commercial Cr etchant, CR-7, for 1 minute. Finally, the HS ribbon microdevices were suspended using the same procedures for releasing control silicon ribbon microdevices. A released HS ribbon microdevice is illustrated in **Figure S2(d)**. We have achieved a yield rate of ~30 % for releasing HS microdevices, as demonstrated in **Figure S5**.
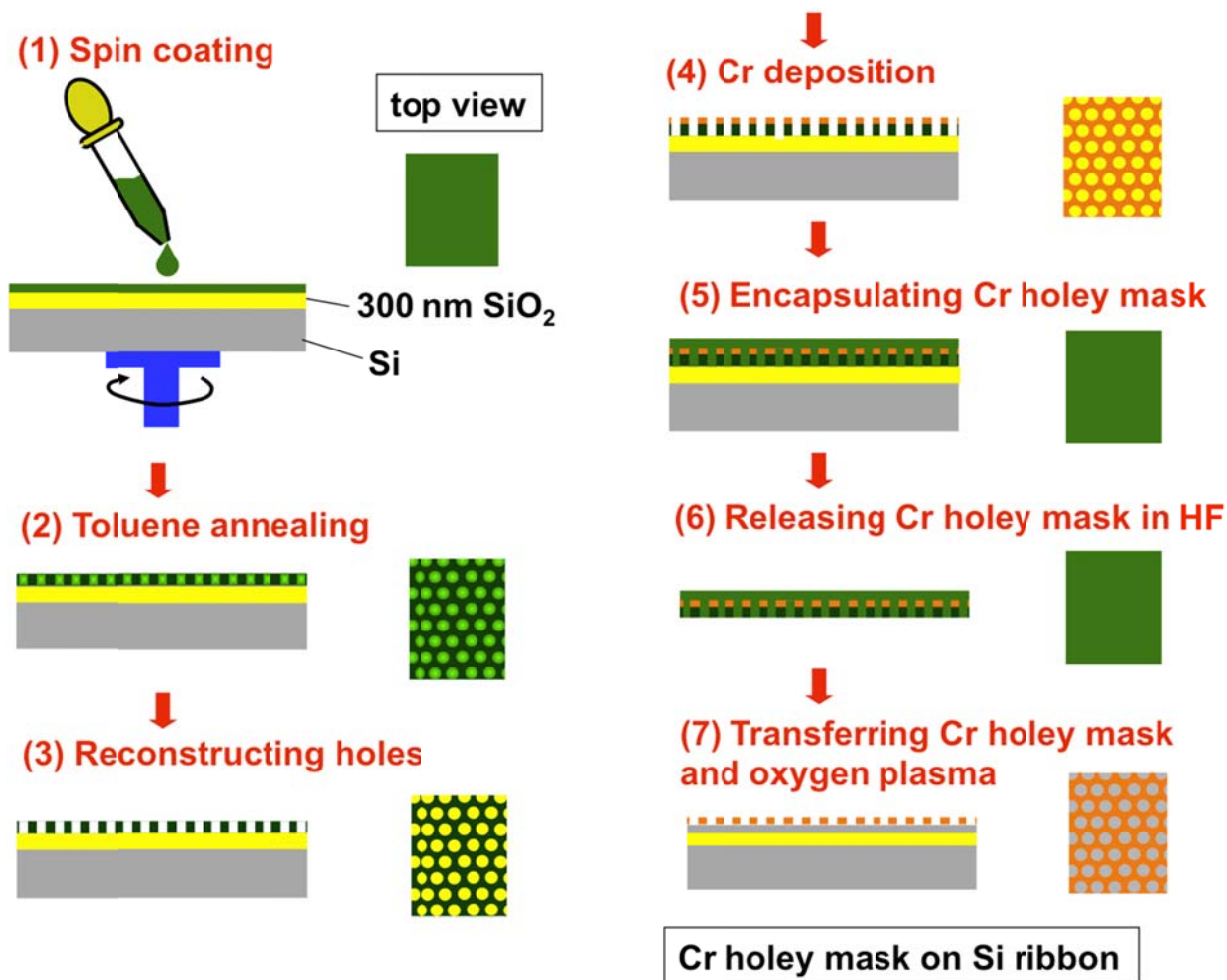
Figure S3. Process flow diagram illustrating the 7 steps of the block copolymer based nanolithography.
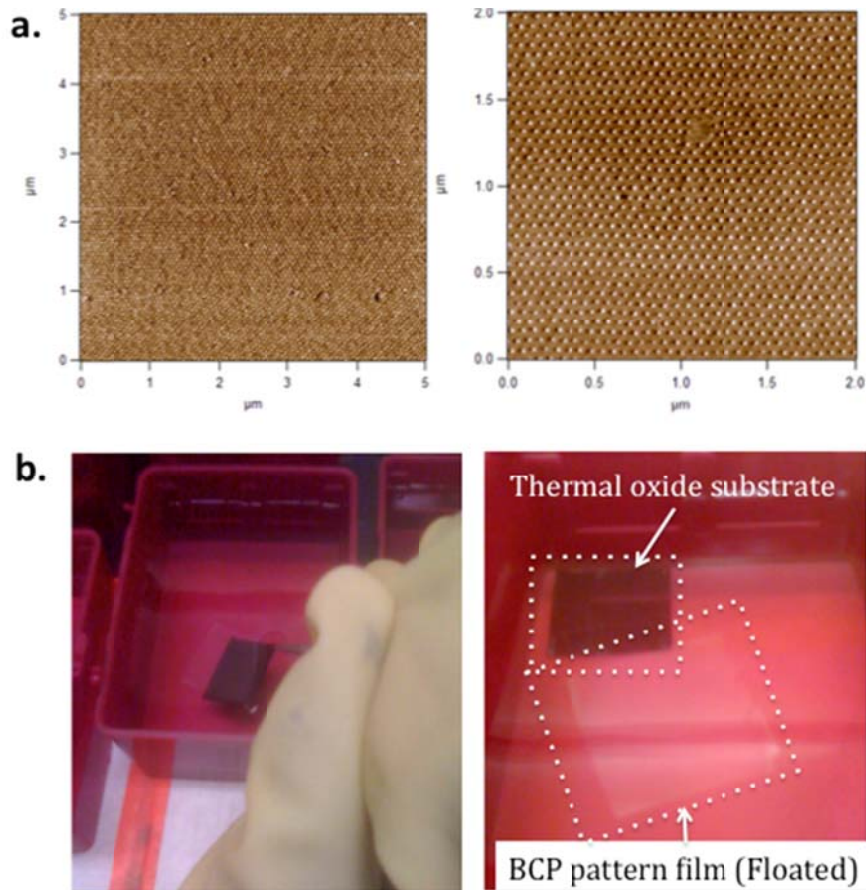
Figure S4. (a) AFM phase images of the block copolymer assembly film. **(b)** Photos during the transfer of the Cr holey mask. The thermal oxide dissolved in the dilated HF bath, causing the 2×2 cm hydrophobic film (*i.e.*, the Cr holey mask encapsulated in the BCP film) floating on the surface of the aqueous bath. The film was then picked up and re-floated in a fresh DI water bath for 5 times to rinse off residual HF. This film was transferred onto the chip with pre-fabricated microdevices.
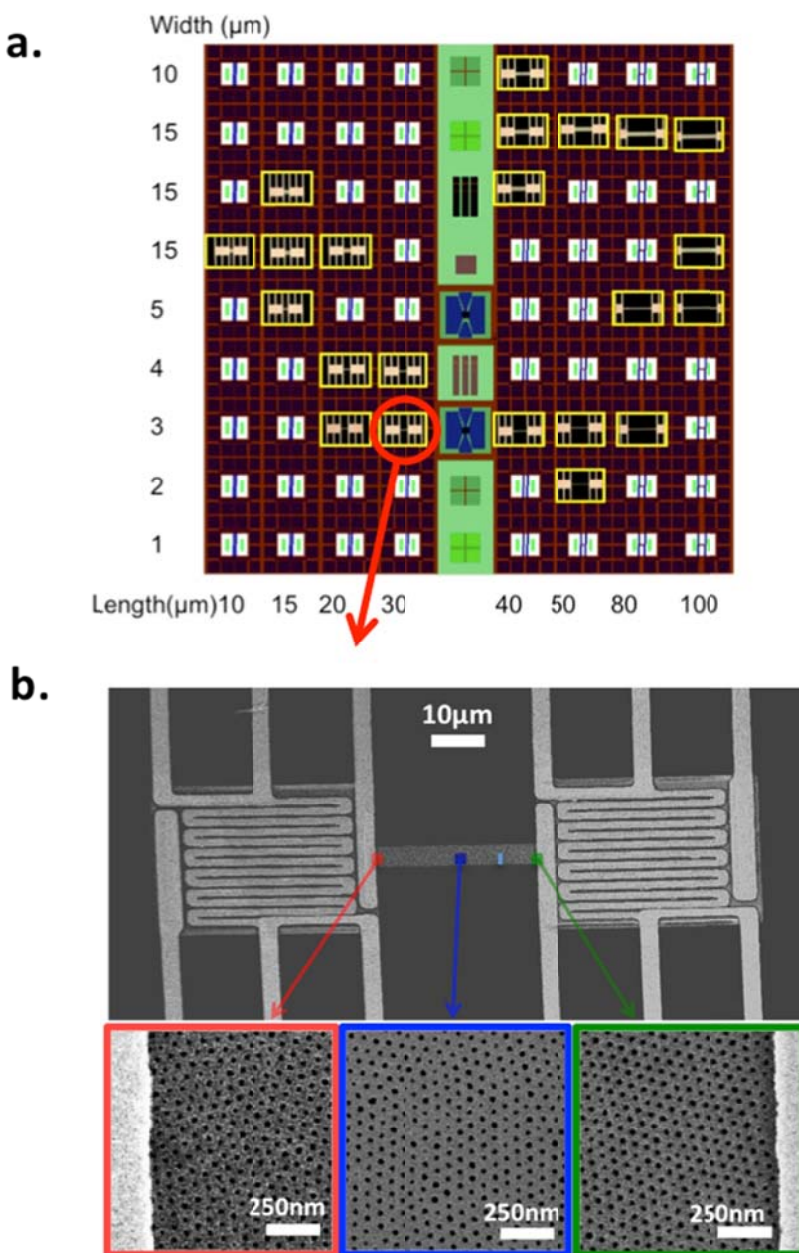
Figure S5. **(a)** L-edit layout of the microdevice chip (~ 8×8 mm), consisting of 8×9 HS microdevices. The optical images of the released HS microdevices are placed on the layout, corresponding to the specific ribbon length and width. For this chip, the yield for releasing HS microdevices is ~30%. **(b)** SEM images of the HS microdevice (ribbon width= 3 μm; length =30 μm) from the same chip. The holey structure was characterized through the entire ribbon to confirm the morphology uniformity. The porosity (~17%) and average neck (35 nm) of this HS ribbon was extracted from the SEM images.

5. Simultaneous Thermoelectric Property Measurements

Thermal conductivity measurement: In **Figure S6(a)**, a DC current (5~10 µA; Keithley 236 Source Measurement Unit) is passed through one PRT on the end-pad to generate a temperature, ΔT_h, above the ambient temperature, T_0, which induces a heat flow through the silicon ribbon to heat the other membrane to ΔT_s. At the same time, a much smaller AC current (~0.5 µA; Lock-in amplifier SR830) are individually passed through the PRTs on the both end-pads to measure the 4-probe electrical resistances, which are then calibrated to be the temperatures of the end-pads given that the electrical conductivity of the PRT is linearly proportional to its temperature. After accounting for the heat loss through the six identical supporting legs to environment and solving the thermal resistance circuit, the thermal conductance through the silicon ribbon is given by

$$G_s = G_b \frac{\Delta T_s}{\Delta T_h - \Delta T_s}$$

$$G_b = \frac{Q_h + Q_L}{\Delta T_h + \Delta T_s}$$

, where G_s and G_b are the thermal conductance of silicon ribbon and supporting legs, respectively. Q_h and $2Q_L$, the Joule heat generated by DC current on the heating PRT and the two supporting legs, respectively, can be calculated from the DC current and the voltage drops across the PRT and the supporting legs.

Seebeck coefficient measurement: During the thermal conductivity measurement shown in **Figure S6(a)**, the open circuit voltage across the inner electrode is also measured (Keithley 2182A nanovoltmeter) under the induced temperature deference. The linear fit to the slope between the voltage and temperature difference is the Seebeck coefficient.

Electrical conductivity measurement: As shown in **Figure S6(b)**, without a temperature gradient across the silicon ribbon, the four-probe electrical conductivity is measured (Keithley 236 Source Measurement Unit) via two inner and outer electrodes.

a. thermal and Seebeck measurement
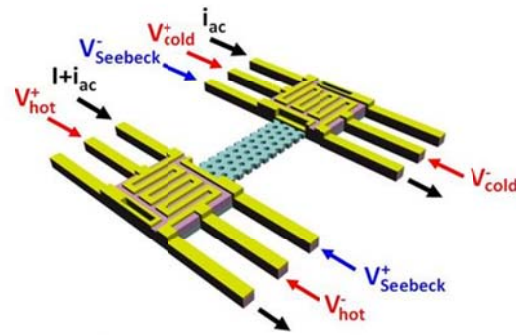
b. 4 probe electrical measurement
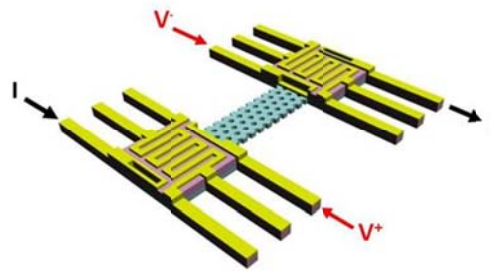
Figure S6. Schematic of the simultaneous thermoelectric property measurements. **(a)** Electrical configuration for the thermal conductivity and Seebeck coefficient measurements. **(b)** Electrical configuration for the electrical conductivity measurement.

6. Electrical Properties with Al_2O_3 Passivation

In **Figure S7**, the conformal coating of Al_2O_3 layer could provide efficient field effect passivation and decrease the surface defect density. After annealing, 5 nm Al_2O_3 layer deposited onto the HS ribbon increased the electrical conductivity by 28% in average.
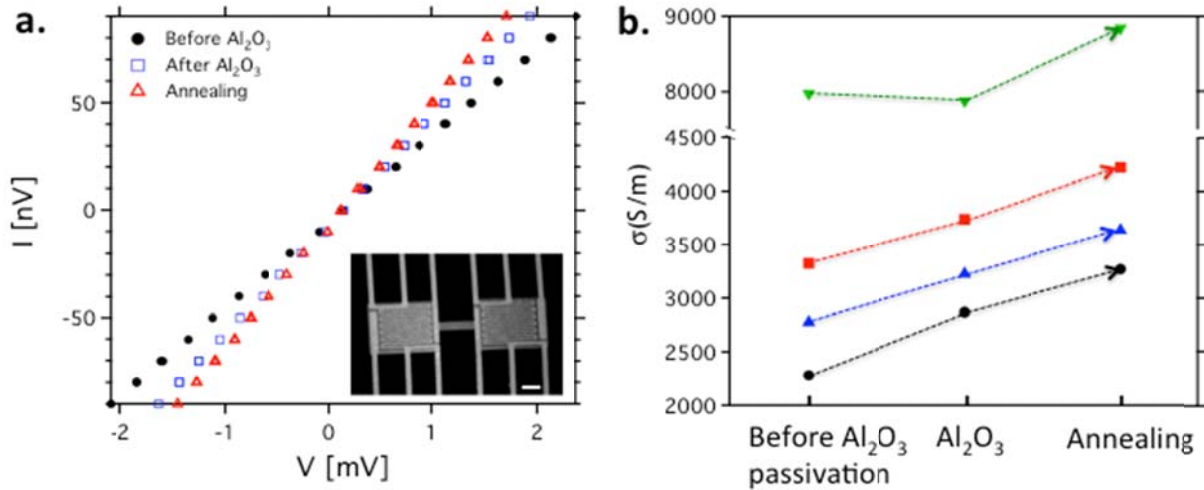
Figure S7. Electrical conductivities of the HS ribbons before and after the Al_2O_3 passivation. The thin Al_2O_3 was deposited by atomic layer deposition (ALD), followed by annealing at 450 °C for 30min in Ar/H_2 gas. **(a)** The 4 probe I-V curve of the HS ribbon with the mid doping and an average neck of ~25 nm. The inset shows the SEM image of the measured HS microdevice with a scale bar of 10μm. **(b)** Change in electrical conductivity for multiple mid-doped HS ribbons. In average, the electrical conductivity increased by 13% after the Al_2O_3 passivation, and by 28% with passivation and annealing combined.

7. Raman Spectroscopy of Holey Silicon and Control Silicon Ribbon

We investigated Raman spectra for HS and control silicon ribbon.[1] Raman spectroscopy has been performed on various silicon nanostructures to investigate phonon localization, anharmonicity and strain effect.[2-6] For example, phonon localization may red-shift and broaden the Raman peak by relaxing fundamental phonon selection rule.[3] RIE etching may creates the nanocrystalline domain at the boundaries, which can be evidenced by red-shifted and broaden Raman spectra.[7] Temperature dependence of the Raman peak shift can represent phonon anharmonicity of HS by perturbation. In this model, the temperature dependence of the phonon frequency is caused by chages of volume and anharmonic phonon-phonon coupling with temperature.[8-11] Hence, the raman frequency as a function of temperature can be given as:[8]

$$\omega(T) = \omega_0 + \Delta(T) ,$$

where ω_0 is harmonic frequency of optical mode of silicon and $\Delta(T)$ accounts for the perturbation of the real part of the phonon self-energy: $\Delta(T) = \Delta^{(1)}(T) + \Delta^{(2)}(T)$, where $\Delta^{(1)}(T)$ is frequency shift due to thermal expansion, and $\Delta^{(2)}(T)$ is frequency shift due to anharmonic phonon-phonon coupling. The slope of frequency with temperature can be approximately expressed with a lattice expansion and an anharmonicity contribution as:[4, 8]

$$\left(\frac{d\omega}{dT}\right) \approx -3\omega_o\gamma\alpha + \frac{k_B}{hc\omega_o}\left[4A + 9B\right] ,$$

where γ, α, A and B are Grüneisen parameter, coefficient of linear thermal expansion, the cubic and quartic anharmonic constants, respectively. Since anharmonic contribution is larger than thermal expansion, the difference in slope between HS and control silicon ribbon can be largely attributed to the difference in Anharmonic constant.[8]

In order to perform Raman spectroscopy, the HS and control ribbon (*i.e.*, without holes) layers were released from the patterned SOI wafer and then transferred onto tungsten coated silicon substrate.[1] In detail, the buried oxide layer was first removed by vapor HF and then the silicon layers were detached and picked up from the substrates by a micromanipulator. Then they were placed on metal coated substrate. Tungsten was chosen because it forms silicide at higher temperature than our measurement. The local temperature change induced by incident laser is subject to the thermal conductance and thermal contact resistance of each sample, and this can lead to variation of Raman spectra. The temperature of samples was carefully controlled by

customized heating stage and the laser power was kept low (6.1 µW, 632.8nm He-Ne laser, 100x 0.9NA objective.) to minimize the local heating. The control ribbon and holey silicon were placed on the same metal substrate at each temperature for consistency.

8. Boltzmann Transport Equation (BTE) Model for Control Silicon Ribbons

In order to understand phonon–impurity scattering in control silicon ribbons, we performed the modeling work and the results is shown in **Figure S8**. Based on kinetic theory derived from the classical Fourier's law, the thermal conductivity accounting for the frequency dependence can be expressed as follows:[12, 13]

$$k = \frac{1}{3} \int \hbar \omega D(\omega) \frac{\partial f(\omega,T)}{\partial T} v(\omega) \Lambda_{eff}(\omega,T) d\omega$$

where $\hbar$ is the reduced Planck constant, f is the Bose-Einstein distribution, D is the density of state ($= D(\kappa) d\kappa / d\omega$), and Λ_{eff} is the effective mean free path followed by $\Lambda_{eff}^{-1} = \Lambda_{imp}^{-1} + \Lambda_{umkl}^{-1} + \Lambda_{bdy}^{-1}$ according to the Matthiessen's rule. Each mean free path is as follows:[14, 15]

$$\Lambda^{-1}_{imp}(\omega) = \frac{A_1 \omega^4}{v_g} \ , \ \Lambda^{-1}_{umkl}(\omega,T) = \frac{B_1 \omega^2 T \exp(-B_2/T)}{v_g} \ , \text{ and } \ \Lambda^{-1}_{bdy} = \left(D \left(\frac{1+p}{1-p} \right) \right)^{-1},$$

where ω, T, D, p, and v_g is the frequency, temperature, film thickness, specularity, and group velocity ($v_g = d\omega / d\kappa$), respectively. In this work, the Born-corn Karman dispersion relation ($\omega = \omega_0 \sin(\pi\kappa/2\kappa_D)$) was used to consider the frequency-dependence, where $\omega_0 = 2v_s \kappa_D / \pi$ and $\kappa_D = (6\pi^2 \eta_{PUC})^{1/3}$ (Debye cutoff wave vector with average sound velocity, v_s) Values of the coefficients A_1, B_1, and B_2 in above equation are summarized in **Table S1** for each lightly, low-, mid-, and high-doped Si sample.

A_1 (impurity scattering constant) values of previous reports and this work are summarized in **Table S2** for thin silicon film with varying doping concentrations.[16-21] A_1 typically ranges 2~5 × 10^{45} (s^3) for a doping concentration of 1.0×10^{18} ~ 1.0×10^{19} cm^{-3} according to the previous experimental and theoretical results. The value of A_1 of our low- and mid-doped silicon control ribbons show 2.4×10^{-45} (s^3) and 4×10^{-45} (s^3), respectively, yielding a good agreement with the previous works.[16-21] The small variances in A_1 between our low-/mid-doped devices and previous reports are within our measurement error. On the other hand, high doping concentration can lead

to significant reduction in thermal conductivity.[16-18, 21] For instance, the previous works show that thermal conductivities of 75 nm thick silicon membranes with concentrations of 3×10^{19} cm^{-3} and 6×10^{19} cm^{-3} are 54 W/mK and 18 W/mK, respectively.[21, 22] This significant reduction may be likely due to unintentional impurities defects, including inactivated dopants, Si interstitials/vacancies, created during ion implantation process. Our data from high-doped device also shows a significant reduction in thermal conductivity. In this study, we used $A_1 = 70 \times 10^{-45}$ (s^3) to fit our high-doped device data and this A_1 value is higher than one estimated based on previous fitting models,[16, 17, 21] suggesting that imperfection during the doping process significantly lowers thermal conductivity as doping concentration increases. Indeed, as-doped sample contains a total dopant concentration up to 4×10^{20} cm^{-3} (calculated by Profile Code, available in **Figure S1(c)**), and yet the carrier concentration acquired after the rapid thermal annealing is only ~6.5×10^{19} cm^3 for the high-doped control ribbon. We simulate impurities and target defects created during ion implantation using SRIM (Stopping and Range of Ions in Matter) package,[23] as presented in the next section.
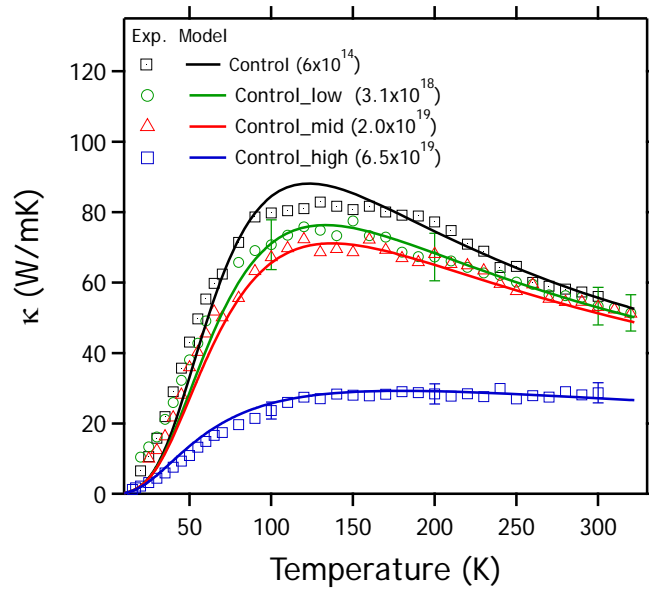
Figure S8. Experimental (marker) and calculated thermal (line) conductivity data of control HS with varying doping concentration.

Table S1. Fitting parameter values used for each sample with respect to different doping level.

	p (0 ≤ p ≤ 1)	A_1 (s^3)	B_1 (s/K)	B_2 (K)
Control, lightly-doped	0.4	1e-48	1.7e-19	210
Control, low-doped	0.4	2.4e-45	1.7e-19	210
Control, mid-doped	0.4	4e-45	1.7e-19	210
Control, high-doped	0.4	7e-44	1.7e-19	210

Table S2. Coefficients for phonon-impurity (boron) scattering rates.

Doping concentration (cm^{-3})	$A_1 \times 10^{45}$ (s^3)
1.0×10^{17} [16]	0.03
1.0×10^{18} [16]	2.06
1.0×10^{19} [16]	5.58
2.0×10^{19} [19, 20]*	20
1.6×10^{21} [17]	144.98
6×10^{14} (this work)	0.001
3.1×10^{18} (this work)	2.4
2.0×10^{19} (this work)	4
6.5×10^{19} (this work)	70

***Experiment and calculation are done in separate groups, and A is fitted to porous structure.**

9. Ion-Atom Collision Events Modeled by SRIM (Stopping and Range of Ions in Matter)

While our thermal conductivity data showed that low- and mid-doped samples do not have a significant effect from defects, high-doped samples likely have a noticeable effect from defects so that its thermal conductivity is lower than low- and mid-doped samples. Using SRIM software package, we simulated collision events under three different ion-implantation doses to understand potential defects and their defect profiles.[23]

In SRIM calculation, we modeled the two-layer structure consisting of 50 nm SiO_2 as the top capping layer and 200 nm Si as the bottom layer. In our HS sample, this bottom silicon layer is the ~100 nm thick device layer of the SOI wafer, and the buried oxide of the SOI wafer is disregarded in SRIM and Profile Code simulations. Ionized boron with an ion energy of 31 keV and a target tilted angle of 7° was selected as the ion source. The above SRIM parameters are identical to those of the Profile Code simulations (**Figure S1**) as well as those of the experimental implantations. To match the experimental ion doses of low-, mid-, and high-doped samples (*i.e.*, 5.0×10^{13}, 5.0×10^{14}, and 5.0×10^{15} cm^{-2}, respectively), SRIM ion counts for an area of 250×250 nm are 31250, 312500, and 3125000, respectively. It should also be noted that the SRIM simulation is performed to study the as-implanted samples, but not for samples after thermal activation.

Figure S9 presents the SRIM results, including the ion-atom depth profiles, the atom distribution depth profiles, and the collision event depth profiles for low-, mid-, high-doped samples. Shown in the ion-atom depth profiles, **Figure S9 (a)~(c)**, each ion collides randomly with target atoms along a random trajectory before it stops. Based on such ion bombardment mechanism,[23] multiple displacement collisions (*i.e.*, collided silicon atom receives energy above its displacement energy) would produce silicon vacancies, silicon interstitials, and silicon-silicon replacement. Shown in the atom distribution depth profiles, **Figure S9 (d)~(f)**, the peaks of boron profiles are deeper than the target (silicon) recoil distribution profiles. Shown in the collision event depth profiles, **Figure S9 (g)~(i)**, it is clear that distributions of target vacancy profile per ion dose (*i.e.*, silicon vacancy, shown in blue) are comparable for low-, mid-, high-doped samples, and vacancy concentration scales with ion dose. These defects will only partially repaired upon post-annealing process and can be a source of impeded electrical conduction in

addition to inactivated dopants (**Figure S1**). We note again that the electrically measured (4-probe) carrier concentration of the high-doped sample (~6.5×10^{19} cm^{-3}) is only ~16% of the expected carrier concentration (~4.0×10^{20} cm^{-3}). This suggests that the thermal activation (1050 °C, 45s in N$_2$ environment) was unable to activate most impurities and/or to repair most target defects to an extent as what were obtained in the low- and mid-doped samples. We also notice that for low- and mid-doped samples, the acquired carrier concentrations are still below the expected carrier concentrations by ~23% and ~52% due to unrepaired defects or inactivated dopants.
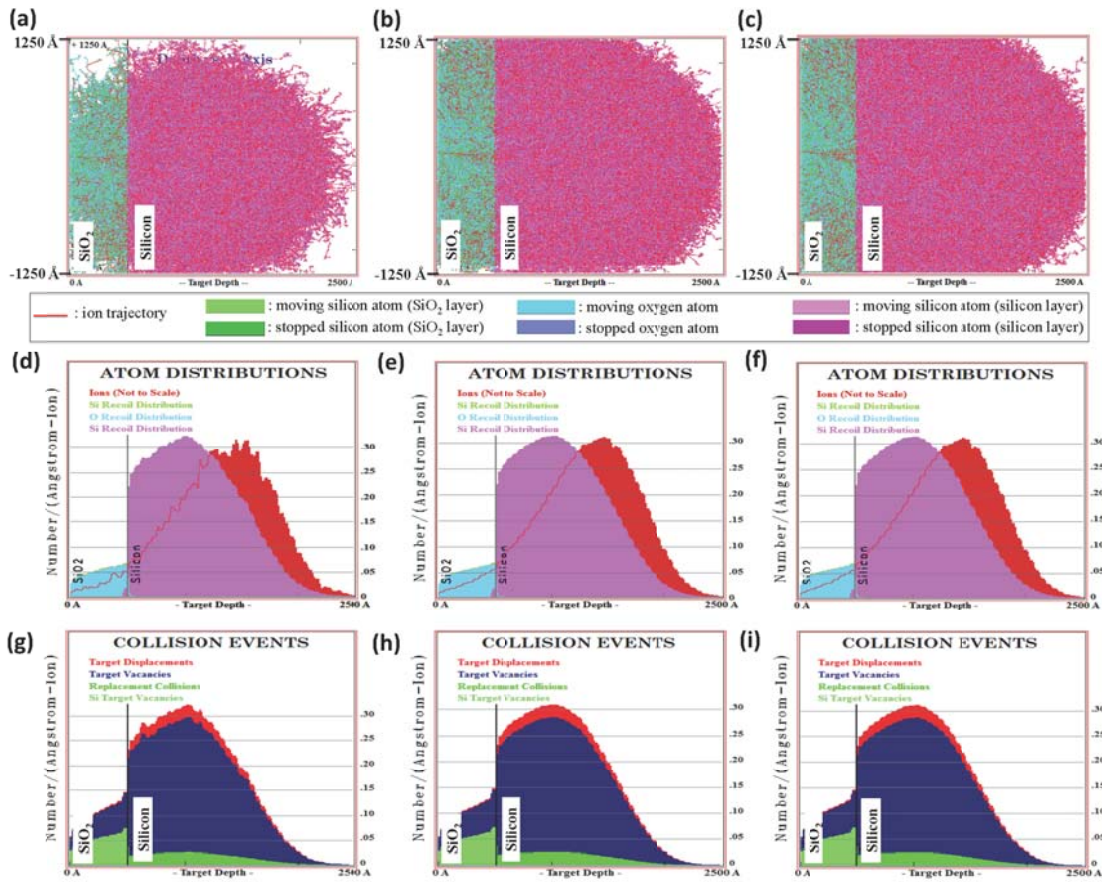
Figure S9. Ion-atom collision simulation using SRIM. (a)~(c) are the ion-atom depth profiles for low-, mid-, high-doped samples. (d)~(f) are the atom distribution depth profiles for low-, mid-, high-doped samples. (g)~(i) are the collision event depth profiles for low-, mid-, high-doped samples. In the silicon bottom layer, silicon vacancy (blue), silicon-silicon replacement (green), and target (silicon) displacement collision (red) are shown in (g)~(i), which follows the two basic principle: (1) displacement collisions = vacancies + replacement collisions, and (2) vacancies = interstitials. The target displacement profiles in (g)~(i) are the same as the silicon recoil distribution profiles in (d)~(f).

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